

09/830360

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

REQUEST FOR FILING NATIONAL PHASE OF J008 Bas'd PCT/PTO  
PCT APPLICATION UNDER 35 U.S.C. 371 AND 37 CFR 1.494 OR 1.495 25 APR 2001To: Hon. Commissioner of Patents  
Washington, D.C. 20231

00909

TRANSMITTAL LETTER TO THE UNITED STATES  
DESIGNATED/ELECTED OFFICE (DO/EO/US)Atty Dkt: P 278095 /7048P-U  
M# /Client Ref.

From: Pillsbury Winthrop LLP, IP Group: Date: April 25, 2001

This is a **REQUEST** for **FILING** a PCT/USA National Phase Application based on:

- |   |                                      |  |
|---|--------------------------------------|--|
| 1. International Application              | 2. International Filing Date         | 3. Earliest Priority Date Claimed  |
| PCT/JP00/05970 ✓<br><u>↑ country code</u> | 1 September 2000 ✓<br>Day MONTH Year | 2 September 1999✓<br>Day MONTH Year<br>(use item 2 if no earlier priority) |
4. Measured from the earliest priority date in item 3, this PCT/USA National Phase Application Request is being filed within:

- (a)  20 months from above item 3 date      (b)  30 months from above item 3 date,  
 (c) Therefore, the due date (unextendable) is May 2, 2001

Title of Invention PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING PRINTED CIRCUIT BOARDInventor(s) INAGAKI, Yasushi et al

Applicant herewith submits the following under 35 U.S.C. 371 to effect filing:

- Please immediately start national examination procedures (35 U.S.C. 371 (f)).  
 A copy of the International Application as filed (35 U.S.C. 371(c)(2)) is transmitted herewith (file if in English but, if in foreign language, file only if not transmitted to PTO by the International Bureau) including:

- a.  Request;  
 b.  Abstract;  
 c. \_\_\_\_\_ pgs. Spec. and Claims;  
 d. \_\_\_\_\_ sheet(s) Drawing which are  informal  formal of size  A4  11"

9.  A copy of the International Application has been transmitted by the International Bureau.

10. A translation of the International Application into English (35 U.S.C. 371(c)(2))

- a.  is transmitted herewith including: (1)  Request; (2)  Abstract;  
 (3) 135 pgs. Spec. and Claims;  
 (4) 53 sheet(s) Drawing which are:  
 informal  formal of size  A4  11"
- b.  is not required, as the application was filed in English.  
 c.  is not herewith, but will be filed when required by the forthcoming PTO Missing Requirements Notice per Rule 494(c) if box 4(a) is X'd or Rule 495(c) if box 4(b) is X'd.  
 d.  Translation verification attached (not required now).

JC08 Rec'd PCT/PTO 25 APR 2001

11.  Please see the attached Preliminary Amendment
12.  Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)), i.e., before 18th month from first priority date above in item 3, are transmitted herewith (file only if in English) including:
13.  PCT Article 19 claim amendments (if any) have been transmitted by the International Bureau
14.  Translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)), i.e., of **claim amendments** made before 18th month, is attached (required by 20th month from the date in item 3 if box 4(a) above is X'd, or 30th month if box 4(b) is X'd, or else amendments will be considered canceled).
15. **A declaration of the inventor** (35 U.S.C. 371(c)(4))  
 a.  is submitted herewith  Original  Facsimile/Copy  
 b.  is not herewith, but will be filed when required by the forthcoming PTO Missing Requirements Notice per Rule 494(c) if box 4(a) is X'd or Rule 495(c) if box 4(b) is X'd.
16. **An International Search Report (ISR):**  
 a. Was prepared by  European Patent Office  Japanese Patent Office  Other  
 b.  has been transmitted by the international Bureau to PTO.  
 c.  copy herewith (1 pg(s).)  plus Annex of family members (1 pg(s).)
17. **International Preliminary Examination Report (IPER):**  
 a.  has been transmitted (if this letter is filed after 28 months from date in item 3) in English by the International Bureau with Annexes (if any) in original language.  
 b.  copy herewith in English.  
 c. 1  IPER Annex(es) in original language ("Annexes" are amendments made to claims/spec/drawings during Examination) including attached amended:  
 c. 2  Specification/claim pages # \_\_\_\_\_ claims #  
 Dwg Sheets #  
 d.  Translation of Annex(es) to IPER (required by 30<sup>th</sup> month due date, or else annexed amendments will be considered canceled).
18. **Information Disclosure Statement** including:  
 a.  Attached Form PTO-1449 listing documents  
 b.  Attached copies of documents listed on Form PTO-1449  
 c.  A concise explanation of relevance of ISR references is given in the ISR.
19.  **Assignment** document and Cover Sheet for recording are attached. Please mail the recorded assignment document back to the person whose signature, name and address appear at the end of this letter.
20.  Copy of Power to IA agent.
21.  **Drawings** (complete only if 8d or 10a(4) not completed): \_\_\_\_\_ sheet(s) per set:  1 set informal;  
 Formal of size  A4  11"
22. Small Entity Status  is Not claimed  is claimed (pre-filing confirmation required)  
 22(a) \_\_\_\_\_ (No.) Small Entity Statement(s) enclosed (since 9/8/00 Small Entity Statements(s) not essential to make claim)
23. **Priority** is hereby claimed under 35 U.S.C. 119/365 based on the priority claim and the certified copy, both filed in the International Application during the international stage based on the filing in (country) JAPAN of:
- | Application No. | Filing Date   | Application No. | Filing Date   |
|-----------------|---------------|-----------------|---------------|
| (1) 11-248311   | Sept. 2, 1999 | (2) 11-369003   | Dec. 27, 1999 |
| (3) 2000-221350 | July 21, 2000 | (4) 2000-230868 | July 31, 2000 |
| (5) 2000-230869 | July 31, 2000 | (6) 2000-230870 | July 31, 2000 |
- a.  See Form PCT/IB/304 sent to US/DO with copy of priority documents. If copy has not been received, please proceed promptly to obtain same from the IB.  
 b.  Copy of Form PCT/IB/304 attached.

09/830360

Page 3 of 4

RE: USA National Phase Filing of PCT/JP00/05970

JC08 Rec'd PCT/PTO 25 APR 2001

24. Attached:

25 Per Item 17.c2, cancel original pages #\_\_\_\_\_, claims #\_\_\_\_\_, Drawing Sheets #26. Calculation of the U.S. National Fee (35 U.S.C. 371 (c)(1)) and other fees is as follows:Based on amended claim(s) per above item(s)  12,  14,  17,  25 (hilite)

Total Effective Claims	77	minus 20 =	57	x \$18/\$9	=	\$1026	966/967
Independent Claims	13	minus 3 =	10	x \$80/\$40	=	\$800	964/965
If any proper (ignore improper) Multiple Dependent claim is present,				add\$270/\$135	+270		968/969

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(4)): →→ BASIC FEE REQUIRED, NOW →→→

A. If country code letters in item 1 are not "US", "BR", "BB", "TT", "MX", "IL", "NZ", "IN" or "ZA"

See item 16 re:

- |  |                 |                     |
|--|-----------------|---------------------|
| 1. Search Report was <u>not</u> prepared by EPO or JPO ----- | add\$1000/\$500 | 960/961             |
| 2. Search Report was prepared by EPO or JPO -----            | add\$860/\$430  | <u>+860</u> 970/971 |

SKIP B, C, D AND E UNLESS country code letters in item 1 are "US", "BR", "BB", "TT", "MX", "IL", "NZ", "IN" or "ZA"

- |  |                   |                      |         |
|--|-------------------|----------------------|---------|
| → <input type="checkbox"/> B. If <u>USPTO</u> did not issue <u>both</u> International Search Report (ISR) <u>and</u> (if box 4(b) above is X'd) the International Examination Report (IPER), -----                           | add\$1000/\$500   | +0                   | 960/961 |
| → <input type="checkbox"/> C. If <u>USPTO</u> issued ISR but not IPER (or box 4(a) above is X'd), -----  | add\$710/\$355    | +0                   | 958/959 |
| → <input type="checkbox"/> D. If <u>USPTO</u> issued IPER but IPER Sec. V boxes <u>not all</u> 3 YES, -----  | add\$690/\$345    | +0                   | 956/957 |
| → <input type="checkbox"/> E. If international preliminary examination fee was paid to <u>USPTO</u> <u>and</u> Rules 492(a)(4) and 496(b) <u>satisfied</u> (IPER Sec. V <u>all</u> 3 boxes YES for <u>all</u> claims), ----- | add \$100/\$50    | +0                   | 962/963 |
| <b>SUBTOTAL = <u>\$2956</u></b>  |                   |                      |         |
| 28. If Assignment box 19 above is X'd, add Assignment Recording fee of ----\$40  | <u>+40</u>        | (581)                |         |
| 29. Attached is a check to cover the -----   | <b>TOTAL FEES</b> | <b><u>\$2996</u></b> |         |

Our Deposit Account No. 03-3975

Our Order No. 41226 | 278095  
C#                  M#                 

00909

**CHARGE STATEMENT:** The Commissioner is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fee(s) filed, or asserted to be filed, or which should have been filed herewith or concerning any paper filed hereafter, and which may be required under Rules 16-18 and 492 (missing or insufficient fee only) now or hereafter relative to this application and the resulting Official document under Rule 20, or credit any overpayment, to our Account/Order Nos. shown above for which purpose a duplicate copy of this sheet is attached.

This CHARGE STATEMENT does not authorize charge of the issue fee until/unless an issue fee transmittal form is filed

Pillsbury Winthrop LLP  
Intellectual Property Group

By Atty: Glenn J. PerryReg. No. 28458

Sig:

Fax:

(202) 822-0944

Tel: (202) 861-3070

Atty/Sec: gjp/mhn

NOTE: File in duplicate with 2 postcard receipts (PAT-103) & attachments.

09/830360

JC08 Rec'd PCT/PTO 25 APR 2001

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re PATENT APPLICATION OF

Inventor(s): INAGAKI, Yasushi et al

Filed: Herewith

Title: PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING PRINTED  
CIRCUIT BOARD

April 25, 2001

**PRELIMINARY AMENDMENT**Hon. Commissioner of Patents  
Washington, D.C. 20231RECEIVED  
U.S. PATENT AND  
TRADEMARK OFFICE  
APR 25 2001

Sir:

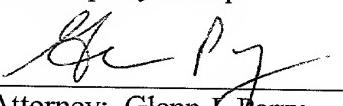
Please amend this application as follows:

**IN THE SPECIFICATION:**

At the top of the first page, just under the title, insert

- This application is the National Phase of International Application  
 PCT/JP00/05970 filed September 1, 2000 which designated the U.S.  
 and that International Application  
 was       was not published under PCT Article 21(2) in English.--

Respectfully submitted,

PILLSBURY WINTHROP LLP  
 Intellectual Property GroupBy: 

Attorney: Glenn J. Perry  
 Reg. No: 28458  
 Tel. No.: (202) 861-3070  
 Fax No.: (202) 822-0944

Atty\Sec. GJP/mhn  
 1100 New York Avenue, NW  
 Ninth Floor  
 Washington, DC 20005-3918  
 (202) 861-3000

## TITLE OF THE INVENTION

PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING PRINTED CIRCUIT BOARD

## 5 Technical Field

The present invention relates to a printed board for mounting thereon electronic components such as an IC chip and a method of manufacturing the printed board. More particularly, the present invention relates to a printed circuit board including therein a capacitor or the like and a method of manufacturing the printed circuit board.

## Background Art

At present, for the purpose of smoothly supplying electric power to an IC chip, a chip capacitor is often mounted on the surface of a printed circuit board used as a package substrate.

The reactance of a wiring from the chip capacitor to the IC chip depends on frequency. Due to this, as IC chip driving frequency increases, the chip capacitor cannot exhibit sufficient effect even if the chip capacitor is mounted on the surface of the printed circuit board. Considering this, the applicant of the present invention proposed a technique, identified as Japanese Patent Application No. 11-248311, for forming a concave portion on a core substrate so as to contain therein a chip capacitor. Techniques for embedding a capacitor in a substrate are disclosed in Japanese Patent Unexamined Application Publication (to be referred to as "Publication" hereinafter) Nos. 6-326472, 7-263619, 10-256429, 11-45955, 11-126978, 11-312868 and the like.

Publication No. 6-326472 discloses a technique for embedding a capacitor in a resin substrate made of glass epoxy. With this constitution, it is possible to reduce power supply

noise and to dispense with a space for mounting the chip capacitor, thereby making an insulating substrate small in size.

Publication No. 7-263619 discloses a technique for embedding a capacitor in a substrate made of ceramic, alumina or the like.

- 5 With this constitution, the capacitor is connected between a power supply layer and a ground layer to thereby shorten wiring length and reduce wiring inductance.

However, according to the Publication Nos. 6-326472 and 7-263619 stated above, the distance from the IC chip to the

- 10 capacitor cannot be set too short and the wiring inductance cannot be reduced as currently desired in the higher frequency region of the IC chip. In case of a multi-layer buildup wiring board made of resin, in particular, due to the difference in the coefficient of thermal expansion and a capacitor made of ceramic and a core substrate as well as interlayer resin insulating layers made of resin, disconnection occurs between the terminal of the chip capacitor and a via, separation occurs between the chip capacitor and the interlayer resin insulating layers and cracks occur to the interlayer resin insulating layers. Thus, the 15 multi-layer buildup wiring board could not realize high reliability for a long time.

- 20 On the other hand, according to the invention of Publication No. 11-248311, if the position at which a capacitor is arranged is deviated, the connection between the terminal of the capacitor and a via cannot be accurately established and power cannot be possibly supplied from the capacitor to the IC chip.

- 25 The present invention has been made to solve the above-stated problems. It is, therefore, an object of the present invention to provide a printed circuit board including therein a capacitor and having enhanced connection reliability and to provide a method of manufacturing the printed circuit

board.

#### Disclosure of the Invention

In order to achieve the above purpose, according to claim 5 1, a printed circuit board constituted by alternately laminating interlayer resin insulating layers and conductive circuits in a multilayer manner on a core substrate containing a capacitor, characterized in that

the core substrate containing said capacitor is 10 constituted by providing a first resin substrate, a second resin substrate having an opening for containing the capacitor and a third resin substrate in a multilayer manner while interposing bonding plates.

According to claim 16, a printed circuit board 15 manufacturing method characterized by comprising at least the following steps (a) to (d) :

(a) forming a conductor pad section on a first resin substrate;  
(b) connecting a capacitor to said conductor pad section of said first resin substrate through a conductive bonding agent;  
20 (c) providing a third resin substrate, a second resin substrate having an opening for containing said capacitor and said first resin substrate in a multilayer manner while interposing bonding plates so that said capacitor of said first resin substrate is contained in said opening of said second resin substrate and that said opening of said second resin substrate is closed by the third resin substrate; and  
25 (d) heating and pressurizing said first resin substrate, said second resin substrate and said third resin substrate, to thereby provide a core substrate.

30 According to a printed circuit board recited in claim 1 and a printed circuit board manufacturing method recited in claim 16, the capacitor can be contained in the core substrate and

the distance between the IC chip and the capacitor is shortened. Therefore, it is possible to reduce the loop inductance of the printed circuit board. Further, since the core substrate is constituted by providing resin substrates in a multilayer manner, 5 it can obtain sufficient strength. Besides, since the core substrate is constituted smoothly by providing the first resin substrate and the third resin substrate on the both sides of the core substrate, respectively, it is possible to appropriately form interlayer resin insulating layers and conductor circuits 10 on the core substrate and to thereby decrease the probability of the occurrence of defective printed circuit boards.

Interlayer resin insulating layers are provided on the core substrate, via holes or through holes are provided in the interlayer resin insulating layers, and conductor circuits serving as conductive layers are formed, which means the circuit 15 is formed by a buildup method. As the buildup method, either a semi-additive method, a full additive method can be employed.

It is preferable that a gap is filled with a resin. By removing the gap between the capacitor and the core substrate, the capacitor included in the core substrate behaves less frequently. Even if a stress resulting from the capacitor occurs, the stress can be eased by the filled resin. Also, the resin can advantageously bond the capacitor to the core substrate and prevent migration. 20

According to claim 2, each of the bonding plates has a core impregnated with a thermosetting resin. Due to this, the core substrate can obtain high strength. 25

According to claim 3, each of the first, second and third resin substrates has a core impregnated with a resin. Due to 30 this, the core substrate can obtain high strength.

According to claim 4, a plurality of capacitors are contained in the core substrate. Due to this, it is possible

to highly integrate the capacitors.

According to claim 5, the conductor circuits are formed on the second resin substrate. Due to this, it is possible to increase the wiring density of the substrate and to reduce the 5 number of interlayer resin insulating layers.

According to claim 6, the capacitor is contained in the substrate and, at the same time, a capacitor is provided on the surface of the printed circuit board. Since the capacitor is contained in the printed circuit board, the distance between 10 the IC chip and the capacitor is shortened, loop inductance is reduced and power can be supplied momentarily. Since the capacitor is also provided on the surface of the printed circuit board, a mass storage capacitor can be attached and high power can be easily supplied to the IC chip.

15 According to claim 7, the capacitance of the capacitor on the surface is equal to or higher than that of a capacitor on an inner layer. Due to this, it is possible to ensure the desired operation of the IC chip without lack of power supply in a high frequency region.

20 According to claim 8, the inductance of the capacitor on the surface is equal to or higher than that of the capacitor on an inner layer. Due to this, it is possible to ensure the desired operation of the IC chip without lack of power supply in a high frequency region.

25 According to claims 9 and 10, the electrode of the chip capacitor on which the metal film is formed is made electrically connectable using a via hole made of a plated material. Here, the electrode of the chip capacitor is made by metalization and has irregular portions on the surface thereof. However, the 30 surface of the chip capacitor is smoothed by the metal film and disconnection does not occur to the electrode, the bonding plates or the like even if a heat cycle test is conducted.

The metal film of the electrode of the capacitor is preferably made of one selected from copper, nickel and noble metal. This is because a layer made of tin or zinc tends to induce migration to the capacitor included in the substrate.

5 For that reason, the metal film can also prevent the occurrence of migration.

Further, the surface of the chip capacitor may be roughed. By doing so, the adhesiveness between the chip capacitor made of ceramic and the bonding layer, the interlayer resin insulating 10 layers made of a resin is high and the separation of the bonding layers and the interlayer resin insulating layers does not occur to interfaces even if a heat cycle test is conducted.

According to claim 11, at least a part of a coating layer of the electrode of the capacitor is exposed and contained in 15 the printed circuit board to thereby make the electrode exposed from the coating layer electrically connectable. In this case, it is preferable that the metal exposed from the coating layer mainly consists of copper. This is because connection resistance can be reduced.

20 According to claim 12, a chip capacitor having electrodes formed inside of an outer edge thereof is employed. Due to this, even if continuity is established through the via hole, a large external electrode can be provided and the allowable range of alignment is widened, so that connection defect can be 25 eliminated.

According to claim 13, a capacitor having electrodes formed in a matrix is employed. Due to this, a large chip capacitor can be contained in the core substrate. Accordingly, capacitance can be increased and electrical problems can be, 30 therefore, solved. Besides, even if going through various heat histories, the printed circuit board does not warp so easily.

According to claim 14, a plurality of chip capacitors for

providing many capacitors may be coupled to be employed as the capacitor. By doing so, it is possible to appropriately adjust capacitance and to appropriately operate the IC chip.

According to claim 15, the coefficient of thermal expansion  
5 of the insulating bonding agent is set lower than that of the containing layer, i.e., set closer to that of the capacitor made of ceramic. Due to this, even if an internal stress resulting from the difference in the coefficient of thermal expansion between the core substrate and the capacitor occurs in a heat  
10 cycle test, cracks, separation and the like less occur to the core substrate, thereby making it possible to attain high reliability.

To obtain the above-stated object, the invention recited in claim 17 is a printed circuit board constituted by providing resin insulating layers and conductor circuits on a core substrate in a multilayer manner, technically characterized in that

the core substrate is constituted by bonding together a plurality of resin substrates, the conductor circuits formed on the plurality of resin substrates; and

a capacitor is contained in the core substrate.

The invention recited in claim 18 is a printed circuit board constituted by providing resin insulating layers and conductor circuit on a core substrate in a multilayer manner,  
25 technically characterized in that

the core substrate is constituted by bonding together a plurality of resin substrates, the conductor circuits formed on the plurality of resin substrates; and

a capacitor is contained in a concave portion formed in  
30 the core substrate.

According to claims 17 and 18, the capacitor can be contained in the core substrate and the distance between the

IC chip and the capacitor is shortened. Due to this, it is possible to reduce the loop inductance of the printed circuit board. In addition, since the core substrate is formed by providing a plurality of resin substrates on which the conductor

5 circuits are formed in a multilayer manner, the wiring density of the core substrate is increased and the number of interlayer resin insulating layers can be reduced.

Interlayer resin insulating layers are provided on the core substrate, via holes or through holes are provided in the

10 interlayer resin insulating layers, and conductor circuits serving as conductive layers are formed, which means a circuit formed by a buildup method. As the buildup method, either a semi-additive method, a full additive method can be employed.

It is preferable that a gap is filled with a resin. By

15 removing the gap between the capacitor and the core substrate, the capacitor included in the core substrate behaves less frequently. Even if a stress resulting from the capacitor occurs, the stress can be eased by the filled resin. Also, the resin can advantageously bond the capacitor to the core substrate and prevent migration.

According to claim 19, a plurality of resin substrates are bonded together with bonding plates interposed therebetween. Due to this, it is possible to strongly bond the resin substrates together.

25 According to claim 20, each of the bonding plates has a core impregnated with a thermosetting resin. Due to this, the core substrate can obtain high strength.

According to claim 21, each of the resin substrates has a core impregnated with a resin. Due to this, the core substrate

30 can obtain high strength.

According to claim 22, a plurality of capacitors are contained in the core substrate. Due to this, it is possible

to highly integrate the capacitors.

According to claim 23, the capacitor is contained in the substrate and, at the same time, a capacitor is provided on the surface of the printed circuit board. Since the capacitor is  
5 contained in the printed circuit board, the distance between the IC chip and the capacitor is shortened, loop inductance is reduced and power can be supplied momentarily. Since the capacitor is also provided on the surface of the printed circuit board, a mass storage capacitor can be attached and high power  
10 can be easily supplied to the IC chip.

According to claim 24, the capacitance of the capacitor on the surface is equal to or higher than that of a capacitor on an inner layer. Due to this, it is possible to ensure the desired operation of the IC chip without lack of power supply  
15 in a high frequency region.

According to claim 25, the inductance of the capacitor on the surface is equal to or higher than that of the chip capacitor on an inner layer. Due to this, it is possible to ensure the desired operation of the IC chip without lack of power supply  
20 in a high frequency region.

According to claims 26 and 27, the electrode of the chip capacitor on which the metal film is formed is made electrically connectable using a via hole made of a plated material. Here, the electrode of the chip capacitor is made by metalization and  
25 has irregular portions on the surface thereof. However, since the surface of the chip capacitor is smoothed by the metal film and the via hole is formed, resin residue does not remain when a through hole is formed in the resin coated on the electrode and the reliability of the connection between the via hole and the electrode can be enhanced. Further, since the via hole is  
30 formed by plating in the electrode having a plated member formed thereon, the characteristics of the connection between the

electrode and the via hole is high and disconnection does not occur between the electrode and the via hole even if a heat cycle test is conducted.

The metal film of the electrode of the capacitor is preferably made of one selected from copper, nickel and noble metal. This is because a layer made of tin or zinc tends to induce migration to the capacitor included in the substrate. For that reason, the metal film can also prevent the occurrence of migration.

Further, the surface of the chip capacitor may be roughed. By doing so, the adhesiveness between the chip capacitor made of ceramic and the bonding layer, the interlayer resin insulating layers made of a resin is high and the separation of the interlayer resin insulating layers does not occur to interfaces even if a heat cycle test is conducted.

According to claim 28, at least a part of a coating layer of the electrode of the capacitor is exposed and contained in the printed circuit board to thereby make the electrode exposed from the coating layer electrically connectable. In this case, it is preferable that the metal exposed from the coating layer mainly consists of copper. This is because high connection characteristics can be ensured and connection resistance can be reduced even if a metal layer is formed by plating on the exposed metal.

According to claim 29, a chip capacitor having electrodes formed inside of an outer edge thereof is employed. Due to this, even if continuity is established through the via hole, a large external electrode can be provided and the allowable range of alignment is widened, so that connection defect can be eliminated.

According to claim 30, a capacitor having electrodes formed in a matrix is employed. Due to this, a large chip capacitor

can be contained in the core substrate. Accordingly, capacitance can be increased and electrical problems can be, therefore, solved. Besides, even if going through various heat histories, the printed circuit board does not warp so easily.

5 According to claim 31, a plurality of chip capacitors for providing many capacitors may be coupled to be employed as the capacitor. By doing so, it is possible to appropriately adjust capacitance and to appropriately operate the IC chip.

10 According to claim 32, the coefficient of thermal expansion of the insulating bonding agent is set lower than that of the core substrate, i.e., set closer to that of the capacitor made of ceramic. Due to this, even if an internal stress resulting from the difference in the coefficient of thermal expansion between the core substrate and the capacitor occurs in a heat cycle test, cracks, separation and the like less occur to the core substrate, thereby making it possible to attain high reliability.

15 According to claim 33, a printed circuit board manufacturing method characterized by comprising at least the following steps (a) to (e):

- (a) forming conductor circuits on a plurality of resin substrates;
- (b) providing a plurality of said resin substrates in a multilayer manner through bonding plates;
- 20 (c) bonding together said resin substrates through said bonding plates, to thereby provide a core substrate;
- (d) forming a concave portion in said core substrate; and
- (e) containing a capacitor in said concave portion.

25 According to claim 34, a printed circuit board manufacturing method comprising at least the following steps (a) to (e):

- (a) forming a resin substrate with a through hole and having

a conductor circuit provided on a surface;

(b) forming a resin substrate without a through hole and having a conductor circuit provided on a surface;

(c) providing said resin substrate with the through hole and

5 said resin substrate without the through hole through a bonding plate in a multilayer manner;

(d) bonding together said resin substrates through said bonding plate, to thereby provide a core substrate; and

(e) containing a capacitor in said concave portion.

10 According to claims 33 and 34, the capacitor can be contained in the core substrate and the distance between the IC chip and the capacitor is shortened. Therefore, it is possible to reduce the loop inductance of the printed circuit board. Also, since the core substrate is formed by providing a plurality of resin substrates, on which conductor circuits are formed, in a multilayer manner, wiring density within the core substrate is increased and the number of interlayer resin insulating layers can be reduced.

15 In order to achieve the above purpose, according to claim 35, a printed circuit board constituted by alternately providing interlayer resin insulating layers and conductor circuits in a multilayer manner on a core substrate containing a capacitor, characterized in that

20 the core substrate containing said capacitor is constituted by providing a first resin substrate, a second resin substrate having an opening for containing the capacitor and a third resin substrate in a multilayer manner while interposing bonding plates; and

25 via holes connected to a terminal of said capacitor are provided on both sides of said core substrate.

According to a printed circuit board recited in claim 35, the capacitor can be contained in the core substrate and the

distance between the IC chip and the capacitor is shortened. Therefore, it is possible to reduce the loop inductance of the printed circuit board. Further, since the core substrate is constituted by providing resin substrates in a multilayer manner, 5 it can obtain sufficient strength. Besides, since the core substrate is constituted smoothly by providing the first resin substrate and the third resin substrate on the both sides of the core substrate, respectively, it is possible to appropriately form interlayer resin insulating layers and conductor circuits 10 on the core substrate and to thereby decrease the probability of the occurrence of defective printed circuit boards. Further, since the via holes are provided on the both sides of the core substrate, it is possible to connect the IC chip to the capacitor and an external connection substrate to the capacitor with 15 shortest distances and it is possible to momentarily supply high power from the external connection substrate to the IC chip.

Interlayer resin insulating layers are provided on the core substrate, via holes or through holes are provided in the interlayer resin insulating layers, and conductor circuits serving as conductive layers are formed, which means the circuit 20 is formed by a buildup method. As the buildup method, either a semi-additive method, a full additive method can be employed.

Further, by arranging connection wirings, it is possible to provide wirings below the capacitor. As a result, the degree 25 of freedom for wirings increases, thereby making it possible to realize high density and make the printed circuit board small in size.

It is preferable that a resin is filled between the capacitor and the substrate. By removing the gap between the 30 capacitor and the substrate, the capacitor included in the core substrate behaves less frequently. Even if a stress resulting from the capacitor occurs, the stress can be eased by the filled

---

resin. Also, the resin can advantageously bond the capacitor to the core substrate and prevent migration.

According to claim 36, each of the bonding plates has a core impregnated with a thermosetting resin. Due to this, the 5 core substrate can obtain high strength.

According to claim 37, each of the first, second and third resin substrates has a core impregnated with a resin. Due to this, the core substrate can obtain high strength. For example, a core impregnated with a reinforcing material such as glass

According to claim 42, the inductance of the capacitor on the surface is equal to or higher than that of the capacitor on an inner layer. Due to this, it is possible to ensure the desired operation of the IC chip without lack of power supply  
5 in a high frequency region.

According to claims 43 and 44, the electrode of the chip capacitor on which the metal film is formed is made electrically connectable using a via hole made of a plated material. Here,  
10 the electrode of the chip capacitor is made by metalization and has irregular portions on the surface thereof. However, since the surface of the chip capacitor is smoothed by the metal film and the via hole is formed, resin residue does not remain when a through hole is formed in the resin coated on the electrode and the reliability of the connection between the via hole and the electrode can be enhanced. Further, since the via hole is  
15 formed by plating in the electrode having a plated member formed thereon, the characteristics of the connection between the electrode and the via hole is high and disconnection does not occur between the electrode and the via hole even if a heat cycle test is conducted.  
20

The metal film of the electrode of the capacitor is preferably made of one selected from copper, nickel and noble metal. This is because a layer made of tin or zinc tends to induce migration to the capacitor included in the substrate.  
25 For that reason, the metal film can also prevent the occurrence of migration.

Further, the surface of the chip capacitor may be roughed. By doing so, the adhesiveness between the chip capacitor made of ceramic and the bonding layer, the interlayer resin insulating  
30 layers made of a resin is high and the separation of the bonding layers and the interlayer resin insulating layers does not occur to interfaces even if a heat cycle test is conducted.

According to claim 45, at least a part of a coating layer of the electrode of the capacitor is exposed and contained in the printed circuit board to thereby make the electrode exposed from the coating layer electrically connectable. In this case,  
5 it is preferable that the metal exposed from the coating layer mainly consists of copper. This is because high connection characteristics can be ensured and connection resistance can be reduced even if a metal layer is formed by plating on the exposed metal.

10 According to claim 46, a chip capacitor having electrodes formed inside of an outer edge thereof is employed. Due to this, even if continuity is established through the via hole, a large external electrode can be provided and the allowable range of alignment is widened, so that connection defect can be  
15 eliminated.

According to claim 47, a chip capacitor having electrodes formed in a matrix is employed. Due to this, a large chip capacitor can be contained in the core substrate. Accordingly, capacitance can be increased and electrical problems can be,  
20 therefore, solved. Besides, even if going through various heat histories, the printed circuit board does not warp so easily.

According to claim 48, a plurality of chip capacitors for providing many capacitors may be coupled to be employed as the capacitor. By doing so, it is possible to appropriately adjust  
25 capacitance and to appropriately operate the IC chip.

According to claim 49, the coefficient of thermal expansion of the insulating bonding agent is set lower than that of the containing layer, i.e., set closer to that of the capacitor made of ceramic. Due to this, even if an internal stress resulting  
30 from the difference in the coefficient of thermal expansion between the core substrate and the capacitor occurs in a heat cycle test, cracks, separation and the like less occur to the

core substrate, thereby making it possible to attain high reliability.

According to claim 50, a printed circuit board manufacturing method characterized by comprising at least the following steps (a) to (d):

- (a) attaching a capacitor to a first resin substrate through a bonding material;
- (b) providing a third resin substrate, a second resin substrate having an opening for containing said capacitor and a first resin substrate in a multilayer manner so that said capacitor of said first resin substrate is contained in said opening of said second substrate and that said opening of said second resin substrate is closed by said third resin substrate, thereby providing a core substrate;
- (c) applying laser and forming a via hole opening reaching said capacitor in said core substrate;
- (d) forming a via hole in said via hole opening.

According to claim 50, the capacitor can be contained in the core substrate and the distance between the IC chip and the capacitor is shortened. Therefore, it is possible to reduce the loop inductance of the printed circuit board.

According to claim 51, a printed circuit board manufacturing method characterized by comprising at least the following steps (a) to (f):

- (a) forming a via hole formation opening in a metal film on one side of a first resin substrate;
- (b) attaching a capacitor to a metal film unformed surface of said first resin substrate through a bonding material;
- (c) providing a third resin substrate, a second resin substrate having an opening for containing said capacitor and said first resin substrate in a multilayer manner by interposing bonding plates so that said capacitor of said first resin substrate is

DRAFTS  
REVISIONS  
FILED  
10

contained in said opening of said second resin substrate and that said opening of said second resin substrate is closed by said third resin substrate;

- (d) heating and pressurizing said first resin substrate, said 5 second resin substrate and said third resin substrate, to thereby provide a core substrate;
- (e) applying laser to said via hole formation opening formed in said metal film of said first resin substrate, and forming a via hole opening reaching said capacitor; and
- 10 (f) forming a via hole in said via hole opening.

According to claim 51, the capacitor can be contained in the core substrate and the distance between the IC chip and the capacitor is shortened. Therefore, it is possible to reduce the loop inductance of the printed circuit board. In addition, 15 an opening is provided in the metal film of the first resin substrate having the metal film formed on one side thereof by etching or the like. By applying laser to the position of the opening, the resin insulating layer exposed from the opening is removed and an opening for a via hole is provided. As a result, 20 the opening diameter of the via hole depends on the opening diameter of the metal film, so that it is possible to form the via hole to have an appropriate opening diameter. Likewise, the positional accuracy of the via hole opening depends on the opening position of the metal film. Due to this, even if the 25 positional accuracy of the laser application is low, it is possible to form the via hole at an appropriate position.

According to claim 52, a printed circuit board manufacturing method characterized by comprising at least the following steps (a) to (f):

- 30 (a) forming via hole formation openings in metal films of a first resin substrate and a third resin substrate, the metal films bonded on one sides of said first resin substrate and said

third resin substrate, respectively;

(b) attaching a capacitor to a metal film unformed surface of said first resin substrate through a bonding material;

(c) providing said third resin substrate, a second resin  
5 substrate having an opening for containing said capacitor and said first resin substrate in a multilayer manner by providing a bonding plate on said metal film unformed surface so that said capacitor of said first resin substrate is contained in said opening of said second resin substrate and that said opening of said second resin substrate is closed by said third resin  
10 substrate;

(d) heating and pressurizing said first resin substrate, said second resin substrate and said third resin substrate, to thereby provide a core substrate;

15 (e) applying laser to said via hole formation openings formed in said first resin substrate and said third resin substrate, and forming a via hole opening reaching said capacitor; and  
(f) forming a via hole in said via hole opening.

According to claim 52, the capacitor can be contained in the core substrate and the distance between the IC chip and the capacitor is shortened. Therefore, it is possible to reduce the loop inductance of the printed circuit board. In addition, openings are provided in the metal films of the first and third resin substrates each having the metal film formed on one side thereof, respectively, by etching or the like. By applying laser to the position of the opening, the resin insulating layer exposed from the opening is removed and an opening for a via hole is provided. As a result, the opening diameter of the via hole depends on the opening diameter of the metal film, so that it is possible to form the via hole to have an appropriate opening diameter. Likewise, the positional accuracy of the via hole opening depends on the opening position of the metal film. Due  
20  
25  
30

to this, even if the positional accuracy of the laser application is low, it is possible to form the via hole at an appropriate position.

Further, since the core substrate is constituted by providing resin substrates in a multilayer manner, it can obtain sufficient strength. Besides, since the core substrate is constituted smoothly by providing the first resin substrate and the third resin substrate on the both sides of the core substrate, respectively, it is possible to appropriately form interlayer resin insulating layers and conductor circuits on the core substrate and to thereby decrease the probability of the occurrence of defective printed circuit boards. Further, since the via holes are provided on the both sides of the core substrate, it is possible to connect the IC chip to the capacitor and an external connection substrate to the capacitor with shortest distances and it is possible to momentarily supply high power from the external connection substrate to the IC chip.

According to claim 53, a printed circuit board manufacturing method characterized by comprising at least the following steps (a) to (g):

- (a) forming a through hole formation openings in metal films of a first resin substrate and a third resin substrate, the metal films bonded on one sides of said first resin substrate and said third resin substrate, respectively;
- (b) attaching a capacitor to a metal film unformed surface of said first resin substrate through a bonding material;
- (c) providing said third resin substrate, a second resin substrate having an opening for containing said capacitor and said first resin substrate in a multilayer manner by providing a bonding plate on said metal film unformed surface so that said capacitor of said first resin substrate is contained in said opening of said second resin substrate and that said opening

of said second resin substrate is closed by said third resin substrate;

(d) heating and pressurizing said first resin substrate, said second resin substrate and said third resin substrate, to thereby provide a core substrate;

(e) applying laser to said through hole formation openings formed in said first resin substrate and said third resin substrate, and forming a via hole opening reaching said capacitor;

10 (f) removing or thinning said metal films; and

(g) forming a conductor circuit and a via hole on said core substrate.

According to claim 53, the capacitor can be contained in the core substrate and the distance between the IC chip and the capacitor is shortened. Therefore, it is possible to reduce the loop inductance of the printed circuit board. In addition, an opening is provided in the metal film of the first resin substrate having the metal film formed on one side thereof by etching or the like. By applying laser to the position of the opening, the resin insulating layer exposed from the opening is removed and an opening for a via hole is provided. Thereafter, the metal film is removed by etching or the like. As a result, the opening diameter of the via hole depends on the opening diameter of the metal film, so that it is possible to form the via hole to have an appropriate opening diameter. Likewise, the positional accuracy of the via hole opening depends on the opening position of the metal film. Due to this, even if the positional accuracy of the laser application is low, it is possible to form the via hole at an appropriate position. In addition, by removing the metal film by etching or the like, wirings can be formed thin and, therefore, formed at fine pitch.

Further, since the core substrate is constituted by

providing resin substrates in a multilayer manner, it can obtain sufficient strength. Besides, since the core substrate is constituted smoothly by providing the first resin substrate and the third resin substrate on the both sides of the core substrate,  
5 respectively, it is possible to appropriately form interlayer resin insulating layers and conductor circuits on the core substrate and to thereby decrease the probability of the occurrence of defective printed circuit boards.

In order to achieve the above purpose, according to claim  
10 54, a printed circuit board constituted by providing resin insulating layers and conductor circuits on a core substrate in a multilayer manner, characterized in that

15 a capacitor is included in said core substrate, and a relatively large lower-layer via hole connected to an electrode of said capacitor is formed; and

20 a plurality of relatively small upper-layer via holes connected to one said lower-layer via hole are provided in an interlayer resin insulating layer on an upper surface of said core substrate.

According to claim 54, a capacitor is included in the core substrate, a relatively large lower-layer via hole connected to a terminal of the capacitor is formed, and a plurality of relatively small upper-layer via holes connected to one the lower-layer via hole are provided in an interlayer resin  
25 insulating layer on an upper surface of the core substrate. By doing so, it is possible to connect the terminal of the capacitor to the lower-layer via holes even if the position at which the capacitor is provided is shifted, and it is possible to ensure the supply of power from the capacitor to the IC chip. Further,  
30 by providing a plurality of relatively small upper-layer via holes, it is possible to obtain the same effect as that of connecting inductances in parallel. Thus, the high frequency

characteristics of power supply lines and ground lines are enhanced, thereby making it possible to prevent the malfunction of the IC chip due to lack of supply of power or the variation of earth level. Moreover, since the wiring length can be  
5 shortened, it is possible to reduce loop inductance.

It is preferable that a concave portion is filled with a resin. By removing the gap between the capacitor and the core substrate, the capacitor included in the core substrate behaves less frequently. Even if a stress resulting from the capacitor  
10 occurs, the stress can be eased by the filled resin. Also, the resin can advantageously bond the capacitor to the core substrate and prevent migration.

According to claims 55 and 56, a filled via hole having a flat surface is employed as the lower-layer via hole. Due to this, it is possible to directly connect a plurality of upper-layer via holes to one lower-layer via hole. Thus, it is possible to enhance the characteristics of the connection between the lower-layer via hole and the upper-layer via hole and to thereby ensure the supply of power from the capacitor  
15 to the IC chip.  
20

According to claim 57, one capacitor is contained in a concave portion formed in the core substrate. Thus, the capacitor is arranged in the core substrate, so that the distance between the IC chip and the capacitor is shortened and it is  
25 possible to reduce the loop inductance of the printed circuit board.

According to claim 58, a plurality of capacitors are contained in the concave portion. Due to this, it is possible to realize the high integration of capacitors.

30 According to claims 59 and 60, the electrode of the chip capacitor on which the metal film is formed is made electrically connectable using a via hole made of a plated material. Here,

the electrode of the chip capacitor is made by metalization and has irregular portions on the surface thereof. However, since the surface of the chip capacitor is smoothed by the metal film and the via hole is formed, resin residue does not remain when  
5 a through hole is formed in the resin coated on the electrode and the reliability of the connection between the via hole and the electrode can be enhanced. Further, since the via hole is formed by plating in the electrode having a plated member formed thereon, the characteristics of the connection between the  
10 electrode and the via hole is high and disconnection does not occur between the electrode and the via hole even if a heat cycle test is conducted.

The surface of the chip capacitor may be roughed. By doing so, the adhesiveness between the chip capacitor made of ceramic and the bonding layer, the interlayer resin insulating layers made of a resin is high and the separation of the bonding layers and the interlayer resin insulating layers does not occur to interfaces even if a heat cycle test is conducted.

According to claim 61, at least a part of a coating layer of the electrode of the capacitor is exposed and contained in the printed circuit board to thereby make the electrode exposed from the coating layer electrically connectable. In this case, it is preferable that the metal exposed from the coating layer mainly consists of copper. This is because high connection  
25 characteristics can be ensured and connection resistance can be reduced even if a metal layer is formed by plating on the exposed metal.

According to claim 62, a chip capacitor having electrodes formed inside of an outer edge thereof is employed. Due to this,  
30 even if continuity is established through the via hole, a large external electrode can be provided and the allowable range of alignment is widened, so that connection defect can be

eliminated.

According to claim 63, a capacitor having electrodes formed in a matrix is employed. Due to this, a large chip capacitor can be contained in the core substrate. Accordingly,  
5 capacitance can be increased and electrical problems can be, therefore, solved. Besides, even if going through various heat histories, the printed circuit board does not warp so easily.

According to claim 64, a plurality of chip capacitors for providing many capacitors may be coupled to be employed as the  
10 capacitor. By doing so, it is possible to appropriately adjust capacitance and to appropriately operate the IC chip.

According to claim 65, a resin is filled between the core substrate and the capacitor, and the coefficient of thermal expansion of the resin is set lower than that of the core substrate,  
15 i.e., set closer to that of the capacitor made of ceramic. Due to this, even if an internal stress resulting from the difference in the coefficient of thermal expansion between the core substrate and the capacitor occurs in a heat cycle test, cracks, separation and the like less occur to the core substrate, thereby  
20 making it possible to attain high reliability.

According to claim 66, a printed circuit board manufacturing method characterized by comprising at least the following steps (a) to (e):

- (a) embedding a capacitor in a core substrate;
- 25 (b) forming a resin insulating layer on an upper surface of said capacitor;
- (c) forming a relatively large lower-layer via hole connected to an electrode of said capacitor, in said resin insulating layer;
- (d) forming an interlayer resin insulating layer on an upper  
30 surface of said core substrate; and
- (e) providing a plurality of relatively small upper-layer via holes connected to one said lower-layer via hole, in said

interlayer resin insulating layer.

According to claim 66, a capacitor is included in the core substrate, a relatively large lower-layer via hole connected to a terminal of the capacitor is formed, and a plurality of 5 relatively small upper-layer via holes connected to one the lower-layer via hole are provided in an interlayer resin insulating layer on an upper surface of the core substrate. By doing so, it is possible to connect the terminal of the capacitor to the lower-layer via even if the position at which the capacitor 10 is provided is shifted, and it is possible to ensure the supply of power from the capacitor to the IC chip. Further, by providing a plurality of relatively small upper-layer via holes, it is possible to obtain the same effect as that of connecting inductances in parallel. Thus, the high frequency 15 characteristics of power supply lines and ground lines are enhanced, thereby making it possible to prevent the malfunction of the IC chip due to lack of supply of power or the variation of earth level. Moreover, since the wiring length can be shortened, it is possible to reduce loop inductance.

According to claim 67, one capacitor is contained in a concave portion formed in the core substrate. Thus, the capacitor is arranged in the core substrate, so that the distance between the IC chip and the capacitor is shortened and it is possible to reduce the loop inductance of the printed circuit 25 board.

According to claim 68, a plurality of capacitors are contained in the concave portion. Due to this, it is possible to realize the high integration of capacitors.

According to claim 69, a through hole is formed in a resin 30 material containing a resin serving as a core material, and a resin material is bonded to the resin material in which the through hole is formed, thereby forming a core substrate having a concave

portion. Due to this, it is possible to form a core substrate having a concave portion which has a flat base.

According to claims 70 and 71, a filled via hole having a flat surface is employed as the lower-layer via hole. Due  
5 to this, it is possible to directly connect a plurality of upper-layer via holes to one lower-layer via hole. Thus, it is possible to enhance the characteristics of the connection between the lower-layer via hole and the upper-layer via hole and to thereby ensure the supply of power from the capacitor  
10 to the IC chip.

According to the invention recited in claim 72, upper surfaces of the plurality of capacitors within the concave portion are pressed or struck from above, thereby making heights of the upper surfaces of the capacitors uniform. Accordingly,  
15 in providing a plurality of capacitors within the concave portion, the heights of the capacitors can be made uniform and the core substrate can be made smooth even if the sizes of the plural capacitors are uneven. Thus, it is possible to appropriately form upper interlayer resin insulating layers and conductor circuits without hampering the smoothness of the core substrate,  
20 and, therefore, to decrease the probability of the occurrence of defective printed circuit boards.

#### Brief Description of Drawings

25 Fig. 1 is a diagram showing a process for manufacturing a printed circuit board according to the first embodiment of the present invention;

30 Fig. 2 is a diagram showing a process for manufacturing the printed circuit board according to the first embodiment of the present invention;

Fig. 3 is a diagram showing a process for manufacturing the printed circuit board according to the first embodiment of

the present invention;

Fig. 4 is a diagram showing a process for manufacturing the printed circuit board according to the first embodiment of the present invention;

5 Fig. 5 is a diagram showing a process for manufacturing the printed circuit board according to the first embodiment of the present invention;

10 Fig. 6 is a diagram showing a process for manufacturing the printed circuit board according to the first embodiment of the present invention;

Fig. 7 is a cross-sectional view of the printed circuit board according to the first embodiment of the present invention;

15 Fig. 8 is a cross-sectional view showing a state in which an IC chip is mounted on the printed circuit board shown in Fig. 7 and that the printed circuit board is attached to a daughter board;

20 Fig. 9 is a cross-sectional view showing a state in which an IC chip is mounted on a printed circuit board according to the first other example of the first embodiment according to the present invention;

Fig. 10 is a diagram showing a process for manufacturing a printed circuit board according to the first modification of the first embodiment of the present invention;

25 Fig. 11 is a cross-sectional view of the printed circuit board according to the first modification of the first embodiment of the present invention;

Fig. 12 is a graph showing the change of the voltage supplied to the IC chip relative to time;

30 Fig. 13 is a cross-sectional view of a chip capacitor contained in the printed circuit board according to the first modification of the first embodiment;

Fig. 14 is a plan view of chip capacitors contained in

a printed circuit board according to the second modification of the first embodiment;

Fig. 15 is a plan view of a chip capacitor contained in the printed circuit board according to the second modification 5 of the first embodiment;

Fig. 16 is a plan view of chip capacitors contained in the printed circuit board according to the second modification of the first embodiment;

Fig. 17 is a view showing a process for manufacturing a 10 printed circuit board according to the second embodiment of the present invention;

Fig. 18 is a view showing a process for manufacturing the printed circuit board according to the second embodiment of the present invention;

15 Fig. 19 is a cross-sectional view of the printed circuit board according to the second embodiment of the present invention;

Fig. 20 is a cross-sectional view showing a state in which 20 an IC chip is mounted on the printed circuit board shown in Fig. 19 and that the printed circuit board is attached to a daughter board;

Fig. 21 is a view showing a process for manufacturing the printed circuit board according to the second embodiment of the present invention;

25 Fig. 22 is a view showing a process for manufacturing the printed circuit board according to the second embodiment of the present invention;

Fig. 23 is a cross-sectional view showing a state in which 30 an IC chip is mounted on the printed circuit board according to the second embodiment of the present invention;

Fig. 24 is a cross-sectional view showing a state in which an IC chip is mounted on a printed circuit board according to

a modification of the second embodiment of the present invention;

Fig. 25 is a view showing a process for manufacturing a printed circuit board according to the third embodiment of the present invention;

5 Fig. 26 is a view showing a process for manufacturing the printed circuit board according to the third embodiment of the present invention;

10 Fig. 27 is a view showing a process for manufacturing the printed circuit board according to the third embodiment of the present invention;

Fig. 28 is a view showing a process for manufacturing the printed circuit board according to the third embodiment of the present invention;

15 Fig. 29 is a view showing a process for manufacturing the printed circuit board according to the third embodiment of the present invention;

Fig. 30 is a cross-sectional view of the printed circuit board according to the third embodiment of the present invention;

20 Fig. 31 is a cross-sectional view showing a state in which an IC chip is mounted on the printed circuit board shown in Fig. 30 and that the printed circuit board is attached to a daughter board;

25 Fig. 32 is a cross-sectional view showing a state in which an IC chip is mounted on a printed circuit board according to a modification of the third embodiment of the present invention;

Fig. 33 is a view showing a process for manufacturing a printed circuit board according to the first modification of the third embodiment of the present invention;

30 Fig. 34 is a view showing a process for manufacturing the printed circuit board according to the first modification of the third embodiment of the present invention;

Fig. 35 is a view showing a process for manufacturing the

printed circuit board according to the first modification of the third embodiment of the present invention;

Fig. 36 is a cross-sectional view of the printed circuit board according to the first modification of the third embodiment of the present invention;

Fig. 37 is a view showing a process for manufacturing a printed circuit board according to the fourth embodiment of the present invention;

Fig. 38 is a view showing a process for manufacturing the printed circuit board according to the fourth embodiment of the present invention;

Fig. 39 is a view showing a process for manufacturing the printed circuit board according to the fourth embodiment of the present invention;

Fig. 40 is a view showing a process for manufacturing the printed circuit board according to the fourth embodiment of the present invention;

Fig. 41 is a view showing a process for manufacturing the printed circuit board according to the fourth embodiment of the present invention;

Fig. 42 is a cross-sectional view of the printed circuit board according to the fourth embodiment of the present invention;

Fig. 43 is a cross-sectional view showing a state in which an IC chip is mounted on the printed circuit board according to the fourth embodiment of the present invention;

Fig. 44(A) is an enlarged view of a via hole 660 shown in Fig. 42 and Fig. 44(B) is a view seen from an arrow B of Fig. 44(A);

Fig. 45 is a view showing a process for manufacturing a printed circuit board according to the first modification of the fourth embodiment of the present invention;

Fig. 46 is a view showing a process for manufacturing the printed circuit board according to the first modification of the fourth embodiment of the present invention;

5 Fig. 47 is a view showing a process for manufacturing the printed circuit board according to the first modification of the fourth embodiment of the present invention;

Fig. 48 is a view showing a process for manufacturing the printed circuit board according to the first modification of the fourth embodiment of the present invention;

10 Fig. 49 is a view showing a process for manufacturing the printed circuit board according to the first modification of the fourth embodiment of the present invention;

15 Fig. 50 is a view showing a process for manufacturing the printed circuit board according to the first modification of the fourth embodiment of the present invention;

Fig. 51 is a view showing a process for manufacturing the printed circuit board according to the first modification of the fourth embodiment of the present invention;

20 Fig. 52 is a cross-sectional view showing a state in which an IC chip is mounted on the printed circuit board according to the first modification of the fourth embodiment of the present invention; and

25 Fig. 53 is a cross-sectional view showing a state in which an IC chip is mounted on the printed circuit board according to the second modification of the fourth embodiment of the present invention.

#### Best Mode for Carrying Out the Invention

##### [First Embodiment]

30 The embodiments of the present invention will be described hereinafter with reference to the accompanying drawings.

First, the constitution of a printed circuit board

according to the first embodiment of the present invention will be described with reference to Figs. 7 and 8. Fig. 7 is a cross-sectional view of a printed circuit board 10 and Fig. 8 shows a state in which an IC chip 90 is mounted on the printed circuit board 10 shown in Fig. 7 and that the printed circuit board 10 is attached to a daughter board 95.

As shown in Fig. 7, the printed circuit board 10 consists of a core substrate 30 containing a plurality of chip capacitors 20 and buildup wiring layers 80A and 80B. Each of the buildup wiring layers 80A and 80B consists of a resin layer 40 and interlayer resin insulating layers 140 and 141. Conductor circuits 58 and via holes 60 are formed on the upper resin layer 40. Conductor circuits 158 and via holes 160 are formed on each of the upper and lower interlayer resin insulating layers 140. Conductor circuit 159 and via holes 164 are formed on each of the upper and lower interlayer resin insulating layers 141. Solder resist layers 70 are formed on the interlayer resin insulating layers 141, respectively. The buildup wiring layers 80A and 80B are connected to each other by way of through holes 56 formed in the core substrate 30.

Each of the chip capacitors 20 consists of the first electrode 21, the second electrode 22 and a dielectric 23 put between the first and second electrodes as shown in Fig. 7. A plurality of pairs of first conductive films 24 connected to the first electrode 21 side and second conductive films 25 connected to the second electrode 22 side are arranged on the dielectric 23 to face one another.

As shown in Fig. 8, solder bumps 76U to be connected to the pads 92P1 and 92P2 of the IC chip 90 are formed on the upper buildup wiring layer 80A. Solder bumps 76D to be connected to the pads 94P1 and 94P2 of the daughter board 95 are formed on the lower buildup wiring layer 80B.

The grounding pad 92P1 of the IC chip 90 is connected to the first electrode 21 of the corresponding chip capacitor 20 through the bump 76U - the conductor circuit 159 - the via hole 164 - the conductor circuit 158 - the via hole 160 - the conductor circuit 58 - the via hole 60. The grounding pad 94P1 of the daughter board 95 is connected to the first electrode 21 of the corresponding chip capacitor 20 through the bump 76D - the via hole 164 - the conductor circuit 158 - the via hole 160 - the through hole 56 - the conductor circuit 58 - the via hole 60.

The power supply pad 92P2 of the IC chip 90 is connected to the second electrode 22 of the corresponding chip capacitor 20 through the bump 76U - the via hole 164 - the conductor circuit 158 - the via hole 160 - the conductor circuit 158 - the via hole 60. The power supply pad 94P2 of the daughter board 95 is connected to the second electrode 22 of the corresponding chip capacitor 20 through the bump 76D - the via hole 164 - the conductor circuit 158 - the via hole 160 - the through hole 56 - the via hole 60. Signal pads of the IC chip are, though not shown, connected to signal pads of the daughter board through the conductor circuits of the printed circuit board, the via holes and the through holes, respectively.

As shown in Fig. 7, the core substrate 30 in this embodiment consists of the first resin substrate 30a having conductive pad sections 34 for connecting the chip capacitors 20 formed on one side, the second resin substrate 30b connected to the first resin substrate 30a through a bonding resin layer (bonding plate) 38a and the third resin substrate 30c connected to the second resin substrate 30b through a bonding resin layer (bonding plate) 38b. An opening 30B capable of containing the chip capacitors 20 is formed in the second resin substrate 30b.

By forming the opening, the chip capacitors 20 can be contained in the core substrate 30. Due to this, the distance

between the IC chip 90 and the chip capacitors 20 is shortened to thereby reduce the loop inductance of the printed circuit board 10. Besides, since the first resin substrate 30a, the second resin substrate 30b and the third resin substrate 30c  
5 are provided in a laminated manner, the core substrate 30 can obtain sufficient strength. Further, since the core substrate 30 is constituted smoothly by providing the first substrate 30a and the third substrate 30c on the both sides of the core substrate 30, respectively, the resin layers 40, 140 and 141 and the  
10 conductor circuits 58, 158 and 159 can be formed on the core substrate 30 appropriately and the probability of the occurrence of defective printed circuit boards can be thereby decreased.

Moreover, in this embodiment, as shown in Fig. 1(D), an insulating bonding agent 33 is interposed between the first resin substrate 30a and each chip capacitor 20. Here, the coefficient of the thermal expansion of the bonding agent 33 is set lower than that of the core substrate 30, i.e., set close to that of the chip capacitors 20 made of ceramic. Due to this, even if an internal stress resulting from the difference in the coefficient of thermal expansion among the core substrate, the bonding layers 40 and the chip capacitors 20, occurs in a heat cycle test, cracks, separation and the like less occur to the core substrate, making it possible to attain high reliability. It is also possible to prevent the occurrence of migration.  
25

A method of manufacturing the printed circuit board described above with reference to Fig. 7 will be described with reference to Figs. 1 to 7.

(1) A copper-clad laminated plate having a copper foil 32 laminated on one side of the first resin substrate 30a having  
30 a core having a thickness of 0.1 mm and made of glass cloth or the like which a BT (Bismaleimide-Triazine) resin is impregnated into and hardened in, is employed as a starting material (Fig.

1 (A) ).

Next, the copper foil 32 side of the copper-clad laminated plate is etched into a pattern, thereby forming conductive pad sections 34 on one side of the first resin substrate 30a (Fig. 5 1(B)).

It is noted that a substrate made of ceramic or AlN cannot be used as the core substrate. This is because such a substrate has poor workability for the outside shape thereof, sometimes cannot contain capacitors and has gaps even if filled with a 10 resin.

(2) Then, using a printer, an bonding material 36 such as a solder paste or a conductive paste is applied onto the conductive pad sections 34 (Fig. 1(C)). The pad sections 34 may be subjected to potting in addition to the application of the bonding material. 15 As the solder paste, one of Sn/Pb, Sn/Sb, Sn/Ag and Sn/Ag/Cu can be employed. Then, resin filler 33 is provided between the conductive pads 34 (Fig. 1(D)). By doing so, it is possible to fill the gaps between chip capacitors 20 and the first resin substrate 30a to be described later. Next, a plurality of chip 20 capacitors 20 made of ceramic are disposed on the conductive pad sections 34 and connected to the conductive pad sections 34 through the bonding material 36 (Fig. 2(A)). Either one or a plurality of chip capacitors 20 may be employed; however, if a plurality of chip capacitors 20 are employed, the high 25 integration of capacitors can be realized.

(3) Next, resin layers for bonding (bonding resin layers) 38a and 38b each having a core made of glass cloth or the like and impregnated with an epoxy resin as well as the second resin substrate 30b (having a thickness of 0.4 mm) and the third resin 30 substrate 30c (having a thickness of 0.1 mm) each having a core made of glass cloth or the like which a BT resin is impregnated into and hardened in, are prepared. Through holes 38A and 30B

capable of containing the chip capacitors 20 are formed in the bonding resin layer 38a and the second resin substrate 30b, respectively. First, the second resin substrate 30b is mounted on the third resin substrate 30c through the bonding resin layer 38b. Next, the first resin substrate 30a is inverted and mounted on the second resin substrate 30b through the bonding resin layer 38a. Namely, the first resin substrate 30a is superposed on the second resin substrate 30b so that the chip capacitors 20 connected to the first resin substrate 30a can be directed toward the bonding resin layer 38a side and can be contained in the through holes formed in the second resin substrate 30b (Fig. 2(B)). By doing so, the chip capacitors 20 can be contained in the core substrate 30 and the printed circuit board having reduced loop inductance can be provided.

(4) The superposed substrates are pressurized using a thermal press, thereby integrating the first, second and third resin substrates 30a, 30b and 30c in a multilayer manner and forming the core substrate 30 having a plurality of chip capacitors 20 (Fig. 2(C)). First, by pressurizing the substrates, the epoxy resin (insulating resin) is pushed outside of the bonding resin layers 38a and 38b and the gaps between the opening 30B and the chip capacitors 20 are filled with the resin. Further, since the substrates are pressurized and, at the same time, heated, the epoxy resin is hardened and the first resin substrate 30a, the second resin substrate 30b and the third resin substrate 30c are fixedly bonded to one another by interposing the bonding resin layers 38a and 38b as bonding resin. In this embodiment, the gaps within the opening 30B are filled with the epoxy resin flowing out of the bonding resin layers. Alternatively, filler can be provided in the opening 30B.

Since the both sides of the core substrate 30 are the first resin substrate 30a and the third resin substrate 30c which are

smooth, respectively, the resin layer 40 and the conductor circuits 58 can be appropriately formed in steps to be described later without damaging the smoothness of the core substrate 30 and the probability of the occurrence of defective printed circuit boards can be decreased. Further, the core substrate 30 can obtain sufficient strength.

(5) Thermosetting epoxy resin sheets to be described later are laminated by vacuum pressing onto the substrate 30 which has been subjected to the above-stated steps, at a pressure of 5 kg/cm<sup>2</sup> while raising temperature to 50 to 150°C to thereby provide interlayer resin insulating layers 40 (Fig. 2(D)). The degree of vacuum during vacuum pressing is 10 mmHg.

(6) Next, openings 42 for via holes reaching the conductive pad sections 34 are formed in the interlayer resin insulating layer 40 at the first resin substrate 30a side and the first resin substrate 30a by applying laser (Fig. 3(A)).

(7) Then, penetrating holes 44 for through holes are formed in the core substrate 30 by drilling or applying laser (Fig. 3(B)). Thereafter, a de-smear process is performed using oxygen plasma. Alternatively, a de-smear process using chemicals such as permanganate may be performed.

(8) Using SV-4540 manufactured by ULVAC JAPAN, Ltd., a plasma process is performed to form rough surfaces 46 on the entire surfaces of the core substrate 30. The plasma process is performed for two minutes while using, as inert gas, argon gas on conditions of power of 200 W, a gas pressure of 0.6 Pa and a temperature of 70°C. Then, sputtering is performed with Ni and Cu as targets and Ni-Cu metal layers 48 are formed on the surfaces of the interlayer resin insulating layers 40, respectively (Fig. 3(C)). While sputtering is employed herein, metal layers of copper, nickel or the like may be formed by electroless plating. In some cases, after performing

sputtering, electroless plated films may be formed. A roughing process may be performed using an acid or an oxidizer. The rough layers are preferably 0.1 to 5  $\mu\text{m}$  thick.

(9) Next, photosensitive dry films are bonded to the surfaces

5 of the Ni-Cu metal layers 48 and exposure and development processes are performed while mounting masks, thereby forming resists 50 each having a predetermined pattern (Fig. 3(D)). The core substrate 30 is immersed in an electroplating solution, current is applied to the core substrate 30 through the Ni-Cu  
10 metal layers 48 and electroplating is conducted to portions in which the resists 50 are not formed on the following conditions, thereby forming electroplated films 52 (Fig. 4(A)).

[Electroplating Solution]

Sulfuric acid	2.24 mol/l
Copper sulfate	0.26 mol/l
Additive (Kaparacid HL manufactured by Atotech Japan	19.5 mol/l

15 [Electroplating Conditions]

Current density	1 A/dm <sup>2</sup>
Duration	120 minutes
temperature	22±2°C

(10) After separating and removing the resists 50 with 5% NaOH, the Ni-Cu metal layers 48 under the resists 50 are dissolved  
20 and removed by etching with a solution mixture of a nitric acid, a sulfuric acid and hydrogen peroxide, thereby forming through holes 56 and conductor circuits 58 (including via holes 60) each consisting of the Ni-Cu metal layer 48 and the electroplated film 52 and having a thickness of 16  $\mu\text{m}$ . After washing and drying  
25 the resultant substrate, an etching solution is sprayed on the

both sides of the substrate and the surfaces of the through holes 56 and the conductor circuits 58 (including the via holes 60) are etched, thereby forming rough layers 62 on the entire surfaces of the through holes 56 and the conductor circuits 58 (including the via holes 60) (Fig. 4(B)). As the etching solution, a mixture of 10 parts by weight of an imidazole copper (II) complex, 7 parts by weight of a glycolic acid, 5 parts by weight of potassium chloride and 78 parts by weight of ion-exchange water is employed.

5 (11) Resin filler 64 mainly consisting of an epoxy resin is filled in the through holes 56, and heated and dried (Fig. 4(C)).

(12) Then, the thermosetting epoxy resin sheets used in the step of (5) are laminated on the substrate by vacuum pressing at a pressure of 5 kg/cm<sup>2</sup> while raising temperature to 50 to 150°C, thereby providing interlayer resin insulating layers 140 (Fig. 4(D)). The degree of vacuum during vacuum pressing is 10 mmHg.

(13) Openings 142 for via holes are then formed in the interlayer resin insulating layers 140 by applying laser (Fig. 5(A)).

(14) Thereafter, by repeating the steps of (8) to (10), conductor circuits 158 (including via holes 160) each consisting of the Ni-Cu metal layer 148 and the electroplated film 152 and having a thickness of 16 µm, and rough surfaces 158α are formed on each of the interlayer resin insulating layers 140 (Fig. 5(B)).

20 (15) By further repeating the steps of (12) to (14), interlayer resin insulating layers 141, conductor circuits 159 (including via holes 164) and rough surfaces 159α are formed further above (Fig. 5(C)).

(16) Next, 46.67 parts by weight of oligomer (having a molecular weight of 4000) which is obtained by forming 50% of epoxy groups 30 of 60 wt% cresol novolac epoxy resin (manufactured by Nippon Kayaku Co., Ltd.) dissolved in diethylene glycol dimethyl ether (DMDG) into an acrylic structure and which imparts photosensitive

characteristic, 15 parts by weight of 80 wt% bisphenol A epoxy resin (Epicoat 1001 manufactured by Yuka Shell) dissolved in methyl ethyl ketone, 1.6 parts by weight of an imidazole hardening agent (2E4MZ-CN manufactured by Shikoku Chemicals Corp.), 3 parts by weight of polyhydric acrylic monomer which is photosensitive monomer (R604 manufactured by Kyoei Chemical), 1.5 parts by weight of polyhydric acrylic monomer (DPE6A manufactured by Kyoei Chemical) and 0.71 parts by weight of a dispersing deforming agent (S-65 manufactured by SANNOPCO) are put in a container, 5 stirred and mixed with one another to prepare a mixture composition. Then, 2.0 parts by weight of benzophenone (manufactured by KANTO KAGAKU) serving as a photoinitiator and 0.2 parts by weight of Michler's ketone (manufactured by KANTO KAGAKU) serving as a photosensitizer are added to the resultant 10 mixture, thereby obtaining a solder resist composition (organic resin insulating material) having a viscosity adjusted to 2.0 Pa·s at 25°C.

The viscosity is measured by a B-type viscometer (DVL-B type manufactured by Tokyo Keiki Co., Ltd.) with a rotor No. 20 4 for 60 rpm and a rotor No. 3 for 4.6 rpm.

(17) Next, the said solder resist composition is applied to each side of the substrate 30 to have a thickness of 20 µm and dried at 70°C for 20 minutes and 70°C for 30 minutes. Thereafter, while photomasks each of which has a thickness of 5 mm and on 25 which the pattern of solder resist opening portions are drawn, are made hermetic contact with the solder resist layers 70, respectively, exposed to ultraviolet rays of 1000 mJ/cm<sup>2</sup>, developed with a DMTG solution, thereby forming openings 71U and 71D (Fig. 6(A)).

(18) Then, the substrate on which the solder resist layers (organic resin insulating layers) 70 have been formed are 30 immersed in an electroless nickel plating solution containing

nickel chloride ( $2.3 \times 10^{-1}$  mol/l), sodium hypophosphite ( $2.8 \times 10^{-1}$  mol/l) and sodium citrate ( $1.6 \times 10^{-1}$  mol/l) and having a pH of 4.5 for 20 minutes to form nickel plated layers 72 each having a thickness of 5  $\mu\text{m}$ , on the opening portions 71U and 71D,  
5 respectively. Further, the substrate is immersed in an electroless plating solution containing potassium gold cyanide ( $7.6 \times 10^{-3}$  mol/l), ammonium chloride ( $1.9 \times 10^{-1}$  mol/l), sodium citrate ( $1.2 \times 10^{-1}$  mol/l) and sodium hypophosphite ( $1.7 \times 10^{-1}$  mol/l) on conditions of 80°C for 7.5 minutes to form gold plated  
10 layers 74 each having a thickness of 0.03  $\mu\text{m}$ , on the nickel plated layers 72, respectively (Fig. 6(B)).

(19) Thereafter, a solder paste is printed on each of the openings 71U and 71D of the solder resist layers 70 and a reflow process is conducted at 200°C, thereby forming solder bumps (solder bodies) 76U and 76D. Consequently, it is possible to obtain the printed circuit board 10 having the solder bumps 76U and 76D (Fig. 7).

Next, description will be given to the mounting of the IC chip 90 on the printed circuit board 10 completed through the above-stated steps and to the attachment of the printed circuit board 10 to the daughter board 95, with reference to Fig. 8. The IC chip 90 is mounted on the printed circuit board 10 thus completed so that the solder pads 92P1 and 92P2 of the IC chip 90 correspond to the solder bumps 76U of the printed  
20 circuit board 10 and a reflow process is performed, thereby attaching the IC chip 90 to the printed circuit board 10. Likewise, a reflow process is performed so that the pads 94P1 and 94P2 of the daughter board 95 correspond to the solder bumps 76D of the printed circuit board 10, thereby attaching the printed  
25 circuit board 10 to the daughter board 95.  
30

The above-stated resin films contain a refractory resin, soluble particles, a hardening agent and other components, each

of which will be described hereinafter.

The resin films employed in the manufacturing method of the present invention has particles soluble in an acid or an oxidizer (to be referred to as "soluble particles" hereinafter) which particles are dispersed in a resin refractory to the acid or the oxidizer (to be referred to as "refractory resin" hereinafter).

The expressions "refractory" and "soluble" will now be described. When materials are immersed in solution composed of the same acid or the same oxidizers for the same time, a material of a type which is dissolved at a relatively high dissolving rate is called a "soluble" material for convenience. A material of a type which is dissolved at a relatively slow dissolving rate is called a "refractory material" for convenience.

The soluble particles are exemplified by resin particles which are soluble in acid or an oxidizer (hereinafter called "soluble resin particles"), inorganic particles which are soluble in acid or an oxidizer (hereinafter called "inorganic soluble particles") and metal particles which are soluble in acid or an oxidizer (hereinafter called "soluble metal particles"). The foregoing soluble particles may be employed solely or two or more particles may be employed.

The shape of each of the soluble particles is not limited. The shape may be a spherical shape or a pulverized shape. It is preferable that the particles have a uniform shape. The reason for this lies in that a rough surface having uniformly rough pits and projections can be formed.

It is preferable that the mean particle size of the soluble particles is  $0.1 \mu\text{m}$  to  $10 \mu\text{m}$ . When the particles have the diameters satisfying the foregoing range, particles having two or more particle sizes may be employed. That is, soluble particles having a mean particle size of  $0.1 \mu\text{m}$  to  $0.5 \mu\text{m}$  and

soluble particles having a mean particle size of 1  $\mu\text{m}$  to 3  $\mu\text{m}$  may be mixed. Thus, a more complicated rough surface can be formed. Moreover, the adhesiveness with the conductor circuit can be improved. In the present invention, the particle size of the soluble particles is the length of a longest portion of each of the soluble particles.

The soluble resin particles may be particles constituted by thermosetting resin or thermoplastic resin. When the particles are immersed in solution composed of acid or an oxidizer, the particles must exhibit dissolving rate higher than that of the foregoing refractory resin.

Specifically, the soluble resin particles are exemplified by particles constituted by epoxy resin, phenol resin, phenoxy resin, polyimide resin, polyphenylene resin, polyolefin resin or fluorine resin. The foregoing material may be employed solely or two or more materials may be mixed.

The soluble resin particles may be resin particles constituted by rubber. Rubber above is exemplified by polybutadiene rubber, a variety of denatured polybutadiene rubber, such as denatured epoxy rubber, denatured urethane rubber or denatured (metha) acrylonitrile rubber, and (metha) acrylonitrile butadiene rubber containing a carboxylic group. When the foregoing rubber material is employed, the soluble resin particles can easily be dissolved in acid or an oxidizer. That is, when the soluble resin particles are dissolved with acid, dissolution is permitted with acid except for strong acid. When the soluble resin particles are dissolved, dissolution is permitted with permanganate which has a relatively weak oxidizing power. When chromic acid is employed, dissolution is permitted even at a low concentration. Therefore, retention of the acid or the oxidizer on the surface of the resin can be prevented. When a catalyst, such as palladium chloride, is supplied after

the rough surface has been formed as described later, inhibition of supply of the catalyst and oxidation of the catalyst can be prevented.

The inorganic soluble particles are exemplified by  
5 particles made of at least a material selected from a group consisting of an aluminum compound, a calcium compound, a potassium compound, a magnesium compound and a silicon compound.

The aluminum compound is exemplified by alumina and aluminum hydroxide. The calcium compound is exemplified by  
10 calcium carbonate and calcium hydroxide. The potassium compound is exemplified by potassium carbonate. The magnesium compound is exemplified by magnesia, dolomite and basic magnesium carbonate. The silicon compound is exemplified by silica and zeolite. The foregoing material may be employed solely or two  
15 or more materials may be mixed.

The soluble metal particles are exemplified by particles constituted by at least one material selected from a group consisting of copper, nickel, iron, zinc, lead, gold, silver, aluminum, magnesium, potassium and silicon. The soluble metal particles may have surfaces coated with resin or the like in  
20 order to maintain an insulating characteristic.

When two or more types of the soluble particles are mixed, it is preferable that the combination of the two types of soluble particles is combination of resin particles and inorganic  
25 particles. Since each of the particles has low conductivity, an insulating characteristic with the resin film can be maintained. Moreover, the thermal expansion can easily be adjusted with the refractory resin. Thus, occurrence of a crack of the interlayer resin insulating layer constituted by the resin  
30 film can be prevented. Thus, separation between the interlayer resin insulating layer and the conductor circuit can be prevented.

The refractory resin is not limited when the resin is able to maintain the shape of the rough surface when the rough surface is formed on the interlayer resin insulating layer by using acid or oxidizer. The refractory resin is exemplified by  
5 thermosetting resin, thermoplastic resin and their composite material. As an alternative to this, the foregoing photosensitive resin of a type having photosensitive characteristic imparted thereto may be employed. When the photosensitive resin is employed, exposure and development  
10 processes of the interlayer resin insulating layers can be performed to form the openings for the via.

In particular, it is preferable that the resin containing thermosetting resin is employed. In the foregoing case, the shape of the rough surface can be maintained against plating solution and when a variety of heating processes are performed.  
15

The refractory resin is exemplified by epoxy resin, phenol resin, phenoxy resin, polyimide resin, polyphenylene resin, polyolefin resin and fluorine resin. The foregoing material may be employed solely or two or more types of the materials  
20 may be mixed.

It is preferable that epoxy resin having two or more epoxy groups in one molecule thereof is employed. The reason for this lies in that the foregoing rough surface can be formed. Moreover, excellent heat resistance and the like can be obtained. Thus,  
25 concentration of stress onto the metal layer can be prevented even under a heat cycle condition. Thus, occurrence of separation of the metal layer can be prevented.

The epoxy resin is exemplified by cresol novolac epoxy resin, bisphenol-A epoxy resin, bisphenol-F epoxy resin, phenol  
30 novolac epoxy resin, alkylphenol novolac epoxy resin, biphenol-F epoxy resin, naphthalene epoxy resin, dicyclopentadiene epoxy resin, an epoxy material constituted by a condensation material

of phenol and an aromatic aldehyde having a phenol hydroxyl group, triglycidyl isocyanurate and alicyclic epoxy resin. The foregoing material may be employed solely or two or more material may be mixed. Thus, excellent heat resistance can be realized.

5 It is preferable that the soluble particles in the resin film according to the present invention are substantially uniformly dispersed in the refractory resin. The reason for this lies in that a rough surface having uniform pits and projections can be formed. When via and through holes are formed  
10 in the resin film, adhesiveness with the metal layer of the conductor circuit can be maintained. As an alternative to this, a resin film containing soluble particles in only the surface on which the rough surface is formed may be employed. Thus, the portions of the resin film except for the surface is not exposed to acid or the oxidizer. Therefore, the insulating characteristic between conductor circuits through the interlayer resin insulating layer can reliably be maintained.  
15

It is preferable that the amount of the soluble particles which are dispersed in the refractory resin is 3 wt% to 40 wt% with respect to the resin film. When the amount of mixture of the soluble particles is lower than 3 wt%, the rough surface having required pits and projections cannot be formed. When the amount is higher than 40 wt%, deep portions of the resin film are undesirably dissolved when the soluble particles are  
20 dissolved by using acid or the oxidizer. Thus, the insulating characteristic between the conductor circuits through the interlayer resin insulating layer constituted by the resin film cannot be maintained. Thus, short circuit is sometimes caused to occur.  
25

30 It is preferable that the resin film contains a hardening agent and other components as well as the refractory resin.

The hardening agent is exemplified by an imidazole

hardening agent, an amine hardening agent, a guanidine hardening agent, an epoxy adduct of each of the foregoing hardening agents, a microcapsule of each of the foregoing hardening agents and an organic phosphine compound, such as triphenylphosphine or  
5 tetraphenyl phosphonium tetraphenyl borate.

It is preferable that the content of the hardening agent is 0.05 wt% to 10 wt% with respect to the resin film. When the content is lower than 0.05 wt%, the resin film cannot sufficiently be hardened. Thus, introduction of acid and the oxidizer into  
10 the resin film occurs greatly. In the foregoing case, the insulating characteristic of the resin film sometimes deteriorates. When the content is higher than 10 wt%, an excessively large quantity of the hardening agent component sometimes denatures the composition of the resin. In the  
15 foregoing case, the reliability sometimes deteriorates.

The other components are exemplified by an inorganic compound which does not exert an influence on the formation of the rough surface and a filler constituted by resin. The inorganic compound is exemplified by silica, alumina and dolomite.  
20 The resin is exemplified by polyimide resin, polyacrylic resin, polyamideimide resin, polyphenylene resin, melanine resin and olefin resin. When any one of the foregoing fillers is contained, conformity of the thermal expansion coefficients can be established. Moreover, heat resistance and chemical resistance  
25 can be improved. As a result, the performance of the printed circuit board can be improved.

The resin film may contain solvent. The solvent is exemplified by ketone, such as acetone, methylethylketone or cyclohexane; aromatic hydrocarbon, such as ethyl acetate, butyl  
30 acetate, cellosolve acetate, toluene or xylene. The foregoing material may be employed solely or two or more materials may be mixed.

[First Other Example of First Embodiment]

A printed circuit board according to the first other example of the first embodiment of the present invention will be described hereinafter with reference to Fig. 9. The printed circuit board in the first other example of the first embodiment is almost the same as the printed circuit board in the first embodiment stated above. However, in the printed circuit board in the first other example, conductive connection pins 96 are provided at the printed circuit board and the printed circuit 5 is connected to a daughter board through the conductive connection pins 96.

10

Further, in the first embodiment stated above, only the chip capacitors 20 contained in the core substrate 30 are provided. In this example, mass storage chip capacitors 86 are mounted 15 on the front and reverse sides of the substrate.

The IC chip momentarily consumes high power and performs complex arithmetic operation. In the first other example, to supply high power to the IC chip, chip capacitors 20 and chip capacitors 86 for power supply are provided. The advantage derived from these chip capacitors will be described with 20 reference to Fig. 12.

Fig. 12 is a graph with a vertical axis indicating voltage supplied to the IC chip and a horizontal axis indicating time. In Fig. 12, two-dot chain line C denotes the voltage variation 25 of a printed circuit board which is not provided with power supply capacitors. If power supply capacitors are not provided, voltage attenuates greatly. A broken line A denotes the voltage variation of a printed circuit board having chip capacitors mounted on the surfaces thereof. Compared with the two-dot chain 30 line C, voltage does not drop greatly. However, since loop length is larger, rate-controlled power supply cannot be conducted sufficiently. Namely, at the start of the supply of power,

voltage falls. Further, a two-dot chain line B denotes the voltage drop of a printed circuit board including the chip capacitors described above with reference to Fig. 8. In this case, loop length can be shortened; however, mass storage chip capacitors cannot be contained in a core substrate 30 and voltage, therefore, varies. Here, a solid line E denotes the voltage variation of the printed circuit board in the first other example which printed circuit board has the chip capacitors 20 mounted in the core substrate and the mass storage chip capacitors 86 mounted on the surfaces thereof. Voltage variation is minimized by providing the chip capacitors 20 and the mass storage chip capacitors 86 (having relatively high inductance) in the vicinity of the IC chip.

15 [First Modification of First Embodiment]

Next, a printed circuit board according to the first modification of the first embodiment of the present invention will be described with reference to Fig. 11.

The printed circuit board in the first modification is almost the same in constitution as the printed circuit board in the above-stated first embodiment. However, in the printed circuit board 14 in the first modification, conductor circuits 35 are formed on one sides of the first resin substrate 30a and the third resin substrate 30c, and conductor circuits 37 are formed on the both sides of the second resin substrate 30b provided with an opening 30B for containing chip capacitors 20. In the first embodiment, the conductor circuits 35 are formed on one sides of the first resin substrate 30a and the third resin substrate 30c and the conductor circuits 37 are formed on the both sides of the second resin substrate 30b. Due to this, it is possible to advantageously increase wiring density and advantageously reduce the number of interlayer resin insulating

layers to be built up.

Furthermore, as shown in Fig. 13(A), in the chip capacitor 20 of the printed circuit board in the first modification, after the coating layer (not shown) of the first and second electrodes 21 and 22 are completely separated, the first and second electrodes 21 and 22 are coated with copper plated films 29. The first and second electrodes 21 and 22 each coated with the copper plated film 29 are electrically connected to each other by a via hole 50 made of a copper plated material. Here, the electrodes 21 and 22 of the chip capacitor are made by metalization and have irregularities on the surfaces thereof. In the first modification, since the surfaces of the first and second electrodes 21 and 22 are smoothed by the copper plated films 29, no migration occurs to thereby cause no disadvantage to the electrodes of the capacitor.

The copper plated films 29 are provided after the nickel / tin layer (coating layer) coated on the surface of each metal layer 26 in a phase of manufacturing chip capacitors 20 is separated in a phase of mounting the chip capacitors on the printed circuit board. Alternatively, the copper plated films 29 can be directly coated on the metal layers 26 in the phase of manufacturing the chip capacitors 20. Namely, in the first modification, as in the case of the first embodiment, after openings reaching the copper plated films 29 of the electrodes are provided by applying laser, a de-smear process is performed to thereby form via holes by copper plating. Accordingly, even if an oxide film is formed on the surface of the copper plated film 29, the oxide film can be removed by the laser and de-smear processes, thereby making it possible to establish connection appropriately.

As shown in Fig. 13(B), it is also possible to employ the first and second electrodes 21 and 22 of the capacitor 20 while

removing part of the coats 28 of the electrodes 21 and 22. This is because connection characteristics can be enhanced by exposing the first and second electrodes 21 and 22.

Further, rough layers 23 $\alpha$  are provided on the surfaces 5 of a dielectric 23 of the chip capacitor 20 which dielectric is made of ceramic. Due to this, the adhesiveness between the chip capacitor 20 made of ceramic and the first resin substrate 30a made of a resin is high and the first resin substrate 30a is not separated on the interface therebetween even if a heat 10 cycle test is conducted. The rough layers 23 $\alpha$  can be formed by polishing the surfaces of the chip capacitor 20 after sintering them or by roughing the surfaces before sintering them. In the first modification, the surfaces of the capacitor are roughed and the adhesiveness between the capacitor and the resin is thereby enhanced. Alternatively, a silane coupling process can 15 be conducted to the surfaces of the capacitor.

A process of manufacturing the printed circuit board according to the first modification of the present invention will be described hereinafter with reference to Figs. 10 and 20 11.

(1) The first resin substrate 30a having a core having a thickness of 0.1 mm and made of glass cloth or the like which a BT (Bismaleimide-Triazine) resin is impregnated into and hardened in, is prepared. Conductive pad sections 34 are formed 25 on one side of the first resin substrate 30a and conductor circuits 35 are formed on the other side of the substrate 30a. Next, a plurality of chip capacitors 20 are mounted on the conductive pad sections 34 through a bonding agent such as a solder or a conductive paste and connected to the conductive pad sections 30 34 (Fig. 10(A)).

(2) Next, resin layers for bonding (bonding resin layers) 38a, 38b each having a core made of glass cloth or the like and

impregnated with an epoxy resin as well as the second resin substrate 30b (having a thickness of 0.4 mm) and the third resin substrate 30c (having a thickness of 0.1 mm) each having a core made of glass cloth or the like which a BT resin is impregnated  
5 into and hardened in, are prepared. Through holes 38A and 38B capable of containing the chip capacitors 20 are formed in the bonding resin layer 38a and the second resin substrate 30b, respectively. Conductor circuits 37 are formed on the both sides of the second resin substrate 30b and conductor circuits 35 are  
10 formed on one side of the third resin substrate 30c. First, the second resin substrate 30b is mounted on a surface on which the conductor circuits 35 of the third resin substrate 30c are not formed, through the bonding resin layer 38b. The first resin substrate 30a is inverted and mounted on the second resin substrate 30b through the bonding resin layer 38a. Namely, the first resin substrate 30a is superposed on the second resin substrate 30b so that the chip capacitors 20 connected to the first resin substrate 30a can be contained in the opening 30B formed in the second resin substrate 30b (Fig. 10(B)).

20 (3) The superposed substrates are pressurized using a thermal press, thereby integrating the first, second and third resin substrates 30a, 30b and 30c in a multilayer manner and forming the core substrate 30 having a plurality of chip capacitors 20 (Fig. 10(C)). First, by pressurizing the substrates, the epoxy resin (insulating resin) is pushed outside of the bonding resin layers 38a and 38b and the gaps between the opening 30B and the chip capacitors 20 are filled with the resin. Further, since the substrates are pressurized and, at the same time, heated, the epoxy resin is hardened and the first resin substrate 30a,  
25 the second resin substrate 30b and the third resin substrate 30c are fixedly bonded to one another by interposing the bonding resin layers 38a and 38b as bonding resin.

(4) Thermosetting epoxy resin sheets are laminated by vacuum pressing onto the substrate 30 which has been subjected to the above-stated steps, at a pressure of 5 kg/cm<sup>2</sup> while raising temperature to 50 to 150°C to thereby provide interlayer resin insulating layers 40 (Fig. 10(D)). The degree of vacuum during vacuum pressing is 10 mmHg.

(5) Next, openings 42 for via holes to be connected to the conductive pad sections 34 and the conductor circuits 35 and 37 are formed on the upper and lower surfaces of the substrate 30 by applying laser (Fig. 10(E)).

Later steps are the same as those of (7) to (19) in the first embodiment stated above, which description will not be, therefore, given herein.

15 [Second Modification of First Embodiment]

Next, the constitution of a printed circuit board according to the second modification of the first embodiment will be described with reference to Fig. 14.

The printed circuit board in the second modification is almost the same in constitution as the printed circuit board in the first embodiment stated above. They, however, differ in chip capacitors 20 contained in the core substrate 30. Fig. 14 is a plan view of chip capacitors. Fig. 14(A) shows a chip capacitor before being cut for providing a plurality of chip capacitors. In Fig. 14(A), a dashed line denotes a cut line. As shown in Fig. 14(B), in the printed circuit board in the first embodiment stated above, the first electrodes 21 and the second electrodes 22 are provided on the edges of the chip capacitor. Fig. 14(C) shows a chip capacitor before being cut for providing a plurality of chip capacitors in the second modification. In Fig. 14(C), a dashed line denotes a cut line. In the printed circuit board in the second modification, as shown in the plan

view of Fig. 14(D), first electrodes 21 and second electrodes 22 are provided inside of the edges of the chip capacitor.

In the printed circuit board in the second modification, the chip capacitors 20 each having electrodes formed inside of 5 the outer edges thereof are employed, so that mass storage chip capacitors can be employed.

Next, a printed circuit board according to the first other example of the second modification will be described with reference to Fig. 15.

10 Fig. 15 is a plan view of a chip capacitor 20 contained in the core substrate of the printed circuit board according to the first other example. In the first embodiment stated above, a plurality of small storage chip capacitors are contained in the core substrate. In the first other example, by contrast, 15 a large, mass storage chip capacitor 20 is contained in the core substrate. The chip capacitor 20 consists of the first electrodes 21, the second electrodes 22, a dielectric 23, first conductive films 24 connected to the first electrodes 21, second conductive films 25 connected to the second electrodes 22, 20 electrodes 27 which are not connected to the first and second conductive films 24 and 25, for the connection of the upper and lower surfaces of the chip capacitor. The IC chip and the daughter board are connected to each other through the electrodes 27.

25 Since the large chip capacitor 20 is employed in the printed circuit board in the first modification, it is possible to employ a mass storage chip capacitor. Further, since the large chip capacitor 20 is employed, the printed circuit board does not warp even if a heat cycle is performed repeatedly.

30 Next, a printed circuit board according to the second other example of the second modification will be described with reference to Fig. 16. Fig. 16(A) shows a chip capacitor before

being cut for providing a plurality of chip capacitors. In Fig. 16(A), a dashed line denotes an ordinary cut line. Fig. 16(B) is a plan view of the chip capacitors. As shown in Fig. 16(B), a plurality of (or in Fig. 16(B), three) chip capacitors for 5 providing multiple capacitors are coupled to one another and employed as a large capacitor as a whole.

In the second other example, since the large chip capacitor 20 is employed, it is possible to employ a mass storage chip capacitor. Further, since the large chip capacitor 20 is 10 employed, the printed circuit board does not warp even if a heat cycle is performed repeatedly.

In the embodiment stated above, the chip capacitors are built in the printed circuit board. Alternatively, plate-like capacitors each constituted by providing a conductive film on a ceramic plate may be employed instead of the chip capacitors. 15

The manufacturing method in the first embodiment makes it possible to contain the capacitors in the core substrate and to shorten the distance between the IC chip and the capacitors, thereby reducing the loop inductance of the printed circuit board. Further, since the printed circuit board is constituted by 20 providing a plurality of resin layers, the core substrate can obtain sufficient strength. Besides, the first resin substrate and the third resin substrate are provided on the both sides of the core substrate, respectively, thereby constituting the 25 core substrate smoothly. Thus, it is possible to appropriately form interlayer resin insulating layers and conductor circuits on the core substrate and to thereby decrease the probability of the occurrence of defective printed circuit boards.

Moreover, since the resin is filled between the core 30 substrate and the capacitors, a stress resulting from the capacitors or the like can be reduced even if it occurs and no migration occurs. Due to this, there is no fear that the

electrodes of the capacitors are separated from the connection sections of the via holes and dissolved. Thus, it is possible to maintain desired performance even if a reliability test is executed.

- 5        In addition, even if the capacitors are coated with copper, it is possible to prevent the occurrence of migration.

[Second Embodiment]

The constitution of a printed circuit board according to  
10 the second embodiment of the present invention will be described  
hereinafter with reference to Figs. 19 and 20. Fig. 19 is a  
cross-sectional view of a printed circuit board 210. Fig. 20  
shows a state in which an IC chip 290 is mounted on the printed  
circuit board 210 shown in Fig. 19 and that the printed circuit  
board 210 is attached to a daughter board 295.

As shown in Fig. 19, the printed circuit board 210 consists  
of a core substrate 230 containing a chip capacitor 220, and  
buildup wiring layers 280A and 280B. The buildup wiring layers  
280A and 280B are connected to each other by through holes 256.  
Each of the wiring layers 280A and 280B consists of interlayer  
resin insulating layers 240 and 340. At the upper buildup wiring  
layer 280A side, conductor circuits 358 and via holes 260  
connected to the first electrode 221 and the second electrode  
222 of the chip capacitor 220, respectively, are formed on the  
25 interlayer resin insulating layer 240, and conductor circuits  
358 and via holes 360 are formed on the interlayer resin insulating  
layers 340. At the lower buildup wiring layer 280B side,  
conductor circuits 258 are formed on the interlayer resin  
insulating layer 240, and conductor circuits 358 and via holes  
360 are formed on the interlayer resin insulating layer 340.  
Solder resist layers 270 are formed on the interlayer resin  
insulating layers 340 of the buildup wiring layers 280A and 280B,

respectively.

As shown in Fig. 19, the chip capacitor 220 consists of the first electrode 221, the second electrode 222 and a dielectric 23 put between the first and second electrodes. A plurality 5 of pairs of first conductive films 224 connected to the first electrode 221 side and second conductive film 225 connected to the second electrode 222 side are arranged to face one another.

As shown in Fig. 20, solder bumps 276U to be connected to the pads 292E, 292P and 292S of the IC chip 290 are provided 10 on the upper buildup wiring layer 280A. Solder bumps 276D to be connected to the pads 294E, 294P and 294S of the daughter board 295 are provided on the lower buildup wiring layer 280B.

The signal pads 292S of the IC chip 290 shown in Fig. 20 are connected to the signal pads 294S of the daughter board 295 through the bumps 276U - the conductor circuits 358 - the via holes 360 - the through holes 256 - the via holes 360 - the bumps 276D, respectively.

The grounding pad 292E of the IC chip 290 is connected to the first electrode 221 of the chip capacitor 220 through the bump 276U - the via hole 360 - the conductor circuit 258 - the via hole 260. The grounding pad 294E of the daughter board 295 is connected to the first electrode 221 of the chip capacitor 220 through the bump 276D - the via hole 360 - the through hole 256 - the via hole 260.

25 The power supply pad 292P of the IC chip is connected to the second electrode 222 of the chip capacitor 220 through the bump 276U - the via hole 360 - the conductor circuit 258 - the via hole 260. The power supply pad 294P of the daughter board 295 is connected to the second electrode 222 of the chip capacitor 30 220 through the bump 276D - the via hole 360 - the through hole 256 - the via hole 260.

As shown in Fig. 19, the core substrate 230 in this

embodiment consists of the first resin substrate 230a, the second resin substrate 230b connected to the first resin substrate 230a through a bonding resin layer (bonding plate) 238a and the third resin substrate 230c connected to the second resin substrate

5 230b through a bonding resin layer (bonding plate) 238b.

Conductor circuits 235 are formed on the both sides of the first resin substrate 230a, the second resin substrate 230b and the third resin substrate 230c. A concave portion 334 capable of containing the chip capacitor 220 is formed in the core substrate

10 230 by spot facing and the chip capacitor 220 is contained in the concave portion 334.

In this way, the chip capacitor 220 can be contained in the core substrate 230, so that the distance between the IC chip 290 and the chip capacitor 220 becomes short and the loop inductance of the printed circuit board 210 can be reduced. Further, since the core substrate 230 is formed by providing the first, second and third resin substrates 230a, 230b and 230c each having the conductor circuits 235 arranged on the both sides thereof, wiring density within the core substrate 230 increases and the number of interlayer resin insulating layers can be thereby reduced.

Furthermore, as shown in Fig. 18(A), in the second embodiment, an bonding agent 236 is interposed between the lower surface of the through hole 34 of the core substrate 230 and the chip capacitor 220, and resin filler 233 is filled between the side surface of the through hole 237 and the chip capacitor 220. Here, the coefficients of thermal expansion of the bonding agent 236 and the resin filler 233 are set lower than that of the core substrate 230, i.e., set close to that of the chip capacitor 220 made of ceramic. Due to this, even if an internal stress resulting from the difference in the coefficient of thermal expansion occurs between the core substrate 230 and the

chip capacitor 220, cracks, separation and the like less occur to the core substrate 230 and high reliability can be, therefore, attained. It is also possible to prevent the occurrence of migration.

5 Next, a method of manufacturing the printed circuit board described above with reference to Fig. 19 will be described with reference to Figs. 17 to 19.

(1) A copper-clad laminated plate 231M having copper foils 232 laminated on the both sides of resin substrates 231a each 10 having a core having a thickness of 0.3 mm and made of glass cloth or the like which a BT (Bismaleimide-Triazine) resin is impregnated into and hardened in, is employed as a starting material (Fig. 17(A)). The copper foils 232 of the copper-clad laminated plate 231M are etched into a pattern fashion, thereby 15 forming the first, second and third resin substrates 230a, 230b and 230c each having the conductor circuits 235 provided on the both sides thereof (Fig. 17(B)). The second resin substrate 230b is superposed on the third resin substrate 230c through the bonding resin layer 238b having a core made of glass cloth or the like and impregnated with an epoxy resin. Likewise, the 20 first resin substrate 230a is superposed on the second resin substrate 230b through the bonding resin layer 238a (Fig. 17(C)).

It is noted that a substrate made of ceramic or AlN cannot be used as the core substrate. This is because such a substrate 25 has poor workability for the outside shape thereof, sometimes cannot contain a capacitor and has gaps even if filled with a resin.

(2) The superposed substrates are pressurized using a thermal press, thereby integrating the first, second and third resin 30 insulating substrates 230a, 230b and 230c in a multi-layer manner and forming the core substrate 230 (Fig. 17(D)). First, by pressuring the substrates, the epoxy resin (insulating resin)

of the bonding resin layers 238a and 238b is pushed outside and the epoxy resin is made hermetic contact with the first, second and third resin substrates 230a, 230b and 230c. Further, since the substrates are pressurized and, at the same time, heated,  
5 the epoxy resin is hardened and the first resin substrate 230a, the second resin substrate 230b and the third resin substrate 230c are fixedly bonded to one another by interposing the bonding resin layers 238a and 238b as bonding plates.

(3) Next, a concave portion 334 for containing the chip  
10 capacitor 220 is formed in the core substrate 230 by spot facing (Fig. 17(E)). While the concave portion for containing the capacitor is provided by spot facing in this embodiment, a core substrate provided with a container section can be formed by overlaying an insulating resin substrate provided with an opening on an insulating resin substrate without an opening.  
15

(4) Then, using a printer, a thermosetting or UV hardening bonding material 236 is applied onto the base of the concave portion 334 (Fig. 18(A)). Alternatively, potting may be conducted instead of the application of the bonding material.

20 Next, the chip capacitor 220 is mounted on the bonding material 236 (Fig. 18(B)). Either one or a plurality of chip capacitors 220 may be employed; however, if a plurality of chip capacitors 220 are employed, the high integration of capacitors can be realized.

25 (5) Thereafter, a thermosetting resin is filled in the concave portion 334, heated and hardened to thereby form a resin layer 233 (Fig. 18(C)). As the thermosetting resin, an epoxy resin, a phenol resin, a polyimide resin and a triazine resin are preferable. Consequently, the chip capacitor 220 within the  
30 concave portion 334 is fixed and the gap between the chip capacitor 220 and the wall surface of the concave portion 334 is filled with the resin.

(6) Thermosetting epoxy resin sheets to be described later are laminated by vacuum pressing onto the substrate 230 which has been subjected to the above-stated steps, at a pressure of 5 kg/cm<sup>2</sup> while raising temperature to 50 to 150°C to thereby provide interlayer resin insulating layers 240 (Fig. 18(D)).  
5 The degree of vacuum during vacuum pressing is 10 mmHg.

Later steps are the same as those of (7) to (9) in the first embodiment stated above, which description will not be, therefore, given herein.

10 Next, description will be given to the mounting of the IC chip 290 on the printed circuit board 210 completed through the above-stated steps and to the attachment of the printed circuit board 210 to the daughter board 295 with reference to Fig. 20. The IC chip 290 is mounted on the printed circuit board 210 thus completed so that the solder pads 292E, 292P and 292S of the IC chip 290 correspond to the solder bumps 276U of the printed circuit board 210 and a reflow process is performed, thereby attaching the IC chip 290 to the printed circuit board 210. Likewise, a reflow process is performed so that the pads 294E, 294P and 294S of the daughter board 295 correspond to the solder bumps 276D of the printed circuit board 210, thereby attaching the printed circuit board 210 to the daughter board 295.  
15  
20

The thermosetting epoxy resin sheets forming the above-stated interlayer resin insulating layers 240 and 340 each contain a refractory resin, soluble particles, a hardening agent and other components, each of which is the same as that in the first embodiment already described above and will not be described herein.  
25

30 [First Modification of Second Embodiment]

Next, a printed circuit board 212 according to the first

modification of the second embodiment of the present invention will be described with reference to Fig. 23. In the second embodiment stated above, a BGA (ball grid array) is provided. The printed circuit board in the first modification of the second embodiment is constituted into a PGA system for establishing connection through conductive connection pins 296 as shown in Fig. 23.

Further, in the second embodiment stated above, the concave portion 334 for containing the chip capacitor 220 is provided in the core substrate 230 by spot facing to allow the chip capacitor 220 to be contained in the concave portion 334. In the first modification of the second embodiment, the first resin substrate 230a provided with through holes 230A, the second and third resin substrates 230b and 230c which are not provided with through holes are bonded to one another through bonding resin layers (bonding plates) 238a and 238b, thereby forming a core substrate 230 provided with a concave portion 335 containing chip capacitors 220 to allow a plurality of chip capacitors 220 to be contained in the concave portion 335.

A process of manufacturing the printed circuit board according to the first modification of the second embodiment of the present invention will be described hereinafter with reference to Figs. 21 and 22.

(1) A copper-clad laminated plate 231M having copper foils 232 laminated on the both sides of resin substrates 231a each having a core having a thickness of 0.3 mm and made of glass cloth or the like which a BT (Bismaleimide-Triazine) resin is impregnated into and hardened in, is employed as a starting material (Fig. 21(A)). The copper foils 232 of the copper-clad laminated plate 231M are etched into a pattern fashion, thereby forming the second and third resin substrates 230b and 230c each having the conductor circuits 235 provided on the both sides

thereof. Also, the copper foils 232 are etched into a pattern fashion and a through hole 230A is formed, thereby forming the first resin substrate 230a having conductor circuits 235 (Fig. 21(B)). The second resin substrate 230b is superposed on the  
5 third resin substrate 230c through the bonding resin layer (bonding plate) 238b having a core made of glass cloth or the like and impregnated with an epoxy resin. Likewise, the first resin substrate 230a having the through hole 230A formed therein is superposed on the second resin substrate 230b through the  
10 bonding resin layer (bonding plate) 238a having the through hole 238A formed therein (Fig. 21(C)).

(2) The superposed substrates are pressurized using a thermal press, thereby integrating the first, second and third resin insulating substrates 230a, 230b and 230c in a multi-layer manner and forming the core substrate 230 provided with a concave portion 335 for containing chip capacitors 220 (Fig. 21(D)). First, by pressuring the substrates, the epoxy resin (insulating resin) of the bonding resin layers 238a and 238b is pushed outside and the epoxy resin is made hermetic contact with the first, second and third resin substrates 230a, 230b and 230c. Further, since the substrates are pressurized and, at the same time, heated, the first resin substrate 230a, the second resin substrate 230b and the third resin substrate 230c are fixedly bonded to one another by interposing the bonding resin layers 238a and 238b  
25 as bonding plates.

(3) Then, using a printer, thermosetting or UV hardening bonding materials 236 are applied onto the base of the concave portion 335 (Fig. 21(E)). Alternatively, potting may be conducted instead of the application of the bonding materials.  
30 (4) Next, a plurality of chip capacitors 220 are mounted on the bonding material 236 (Fig. 22). By containing a plurality of chip capacitors 220 in the core substrate, the high integration

of capacitors can be realized.

(5) Thereafter, a thermosetting resin is filled between the chip capacitors 220 in the concave portion 335, heated and hardened to thereby form a resin layer 233 (Fig. 22(B)). As the thermosetting resin, an epoxy resin, a phenol resin, a polyimide resin and a triazine resin are preferable.

Consequently, the chip capacitors 220 within the concave portion 335 is fixed and the gaps between the chip capacitors 220 and the wall surface of the concave portion 335 are filled with the resin.

(6) Thermosetting epoxy resin sheets are laminated by vacuum pressing onto the substrate 230 which has been subjected to the above-stated steps, at a pressure of 5 kg/cm<sup>2</sup> while raising temperature to 50 to 150°C to thereby provide interlayer resin insulating layers 240 made of an epoxy resin (Fig. 22(C)).

(7) Next, openings 42 for via holes reaching the first terminals 221 and the second terminals 222 of the chip capacitors 220 are formed in the interlayer resin insulating layer 240 at the resin substrate 230a side by applying laser (Fig. 22(D)).

Later steps are the same as those of (8) to (21) in the first embodiment stated above, which description will not be, therefore, given herein.

[First Other Example of First Modification of Second Embodiment]

Next, a printed circuit board according to the first other example of the first modification of the second embodiment of the present invention will be described with reference to Fig. 24. The printed circuit board in the first other example is almost the same as that in the first modification of the second embodiment stated above. However, only the chip capacitors 220 contained in the core substrate 230 are provided in the first modification of the second embodiment, whereas mass storage chip

capacitors 286 are mounted on the front and reverse sides of a core substrate in the first other example.

An IC chip momentarily consumes high power and performs complex arithmetic operation. Here in this first modification, 5 to supply high power to the IC chip, chip capacitors 220 and chip capacitors 286 for power supply are provided. The advantage derived from these chip capacitors will be described with reference to Fig. 12.

Fig. 12 is a graph with a vertical axis indicating voltage supplied to the IC chip and a horizontal axis indicating time. In Fig. 12, two-dot chain line C denotes the voltage variation of a printed circuit board which is not provided with power supply capacitors. If power supply capacitors are not provided, voltage attenuates greatly. A broken line A denotes the voltage variation of a printed circuit board having chip capacitors mounted on the surfaces thereof. Compared with the two-dot chain line C, voltage does not drop greatly. However, since loop length is larger, rate-controlled power supply cannot be conducted sufficiently. Namely, at the start of the supply of power, 10 voltage falls. Further, a two-dot chain line B denotes the voltage drop of a printed circuit board including the chip capacitors described above with reference to Fig. 23. In this case, loop length can be shortened; however, mass storage chip capacitors cannot be contained in a core substrate 230 and voltage, 15 therefore, varies. Here, a solid line E denotes the voltage variation of the printed circuit board in the modification which printed circuit board has the chip capacitors 220 mounted in the core substrate and the mass storage chip capacitors 286 mounted on the surfaces thereof. Voltage variation is minimized 20 by providing the chip capacitors 220 and the mass storage chip capacitors 286 (having relatively high inductance) in the vicinity of the IC chip.

DRAFT 09/06/2013

Furthermore, as shown in Fig. 13(A), in the chip capacitor 220 of the printed circuit board in the first other example of the second embodiment, after the coating layer (not shown) of the first and second electrodes 221 and 222 are completely separated, the first and second electrodes 221 and 222 are coated with copper plated films 29. The first and second electrodes 221 and 222 each coated with the copper plated film 29 are electrically connected to each other by a via hole 260 made of a copper plated material. Here, the electrodes 221 and 222 of the chip capacitor are made by metalization and have irregular portions on the surfaces thereof. Due to this, if the substrate is used while exposing the metal layers, resin may sometimes remain on the irregular portions in the step of providing non-penetrating holes 242 in the connection layer 240. At this time, the resin residue causes connection defects between the first, second electrodes 221 and 222 and the via holes 260. In the first other example, by contrast, since the surfaces of the first and second electrodes 221 and 222 are smoothed by the copper plated films 29, no resin remains when providing non-penetrating holes 42 in the coated interlayer resin insulating layer 240 on the electrodes and the reliability of the connection between the electrodes 221, 222 and the via holes 260 when forming the via holes 260 can be enhanced.

Furthermore, the via holes 260 are formed by plating in the electrodes 221 and 222 having the copper plated films 29 formed thereon, respectively, the connection characteristics between the electrodes 221, 222 and the via holes 260 is good and disconnection does not occur between the electrodes 221, 222 and the via holes 260 even if a heat cycle test is conducted. Besides, no migration occurs and no disadvantages are derived in the connection portions of the via holes of the capacitors.

The copper plated films 29 are provided after the nickel

/ tin layer (coating layer) coated on the surface of each metal layer 26 in a phase of manufacturing chip capacitors is separated in a phase of mounting the chip capacitors on the printed circuit board. Alternatively, the copperplated films 29 can be directly 5 coated on the metal layers 26 in the phase of manufacturing the chip capacitors 220. Namely, in the first other example, as in the case of the second embodiment, after openings reaching the copper plated films 29 of the electrodes are provided by applying laser, a de-smear process is performed to thereby form 10 via holes by copper plating. Accordingly, even if an oxide film is formed on the surface of the copper plated film 29, the oxide film can be removed by the laser and de-smear processes, thereby making it possible to establish connection appropriately.

Further, rough layers 23 $\alpha$  are provided on the surfaces 15 of a dielectric 23 of the chip capacitors 220 which dielectric is made of ceramic. Due to this, the adhesiveness between the chip capacitors 220 made of ceramic and the interlayer resin insulating layer 240 made of a resin is high and the interlayer resin insulating layer 240 is not separated on the interface 20 therebetween even if a heat cycle test is conducted. The rough layers 23 $\alpha$  can be formed by polishing the surfaces of the chip capacitors 220 after sintering them or by roughing the surfaces before sintering them. In the first other example, the surfaces 25 of the capacitors are roughed and the adhesiveness between the capacitors and the resin is thereby enhanced. Alternatively, a silane coupling process can be conducted to the surfaces of the capacitors.

As shown in Fig. 13(B), it is also possible to employ the first and second electrodes 21 and 22 of the first and second 30 capacitors 220 while removing part of the coats 28 of the electrodes 21 and 22. This is because connection characteristics can be enhanced by exposing the first and second

electrodes 221 and 222.

[Second Modification of Second Embodiment]

Next, the constitution of a printed circuit board according to the second modification of the second embodiment will be  
5 described with reference to Fig. 14.

The printed circuit board in the second modification is almost the same in constitution as the printed circuit board in the first embodiment stated above. They, however, differ in chip capacitors 20 contained in the core substrate 30. Fig.  
10 14 is a plan view of chip capacitors. Fig. 14(A) shows a chip capacitor before being cut for providing a plurality of chip capacitors. In Fig. 14(A), a dashed line denotes a cut line. As shown in Fig. 14(B), in the printed circuit board in the first embodiment stated above, the first electrodes 21 and the second electrodes 22 are provided on the edges of the chip capacitor.  
15 Fig. 14(C) shows a chip capacitor before being cut for providing a plurality of chip capacitors in the second modification. In Fig. 14(C), a dashed line denotes a cut line. In the printed circuit board in the second modification, as shown in the plan view of Fig. 14(D), first electrodes 21 and second electrodes 22 are provided inside of the edges of the chip capacitor.  
20

In the printed circuit board in the second modification, the chip capacitors 20 each having electrodes formed inside of the outer edges thereof are employed, so that mass storage chip capacitors can be employed.  
25

Next, a printed circuit board according to the first other example of the second modification will be described with reference to Fig. 15.

Fig. 15 is a plan view of a chip capacitor 20 contained  
30 in the core substrate of the printed circuit board according to the first other example. In the first embodiment stated above, a plurality of small storage chip capacitors are contained in

the core substrate. In the first other example, by contrast, a large, mass storage chip capacitor 20 is contained in the core substrate. The chip capacitor 20 consists of the first electrodes 21, the second electrodes 22, a dielectric 23, first 5 conductive films 24 connected to the first electrodes 21, second conductive films 25 connected to the second electrodes 22, and electrodes 27 which are not connected to the first and second conductive films 24 and 25, for the connection of the upper and lower surfaces of the chip capacitor. The IC chip and the 10 daughter board are connected to each other through the electrodes 27.

Since the large chip capacitor 20 is employed in the printed circuit board in the first modification, it is possible to employ a mass storage chip capacitor. Further, since the large chip 15 capacitor 20 is employed, the printed circuit board does not warp even if a heat cycle is performed repeatedly.

Next, a printed circuit board according to the second other example of the second modification will be described with reference to Fig. 16. Fig. 16(A) shows a chip capacitor before being cut for providing a plurality of chip capacitors. In Fig. 16(A), a dashed line denotes an ordinary cut line. Fig. 16(B) 20 is a plan view of the chip capacitors. As shown in Fig. 16(B), a plurality of (or in Fig. 16(B), three) chip capacitors for providing multiple capacitors are coupled to one another and 25 employed as a large capacitor as a whole.

In the second other example, since the large chip capacitor 20 is employed, it is possible to employ a mass storage chip capacitor. Further, since the large chip capacitor is employed, the printed circuit board does not warp even if a heat cycle 30 is performed repeatedly.

In the embodiment stated above, the chip capacitors are built in the printed circuit board. Alternatively, plate-like

capacitors each constituted by providing a conductive film on a ceramic plate may be employed instead of the chip capacitors.

As stated above, according to the second embodiment, it is possible to contain the capacitors in the core substrate and 5 to shorten the distance between the IC chip and the capacitors, thereby reducing the loop inductance of the printed circuit board. Further, since the core substrate is formed by providing a plurality of resin substrates having conductor circuits formed thereon in a multilayer manner, the wiring density within the 10 core substrate is increased and the number of interlayer resin insulating layers can be reduced.

Moreover, since the resin is filled between the core substrate and the capacitors, a stress resulting from the capacitors or the like can be reduced even if it occurs and no 15 migration occurs. Due to this, there is no fear that the electrodes of the capacitors are separated from the connection sections of the via holes and dissolved. Thus, it is possible to maintain desired performance even if a reliability test is executed.

20 In addition, even if the capacitors are coated with copper, it is possible to prevent the occurrence of migration.

### [Third Embodiment]

The constitution of a printed circuit board according to 25 the third embodiment of the present invention will be described hereinafter with reference to Figs. 30 and 31. Fig. 30 is a cross-sectional view of a printed circuit board 410. Fig. 31 shows a state in which an IC chip 490 is mounted on the printed circuit board 410 shown in Fig. 30 and that the printed circuit 30 board 410 is attached to a daughter board 495.

As shown in Fig. 30, the printed circuit board 410 consists of a core substrate 430 containing a plurality of chip capacitors

420, and buildup wiring layers 480A and 480B. Each of the buildup wiring layers 480A and 480B consists of interlayer resin insulating layers 540 and 541. Conductor circuits 558 and via holes 560 are formed on the interlayer resin insulating layer 540 of each of the buildup wiring layers 480A and 480B. Conductor circuits 559 and via holes 564 are formed on the interlayer resin insulating layer 541 of each of the buildup wiring layers 480A and 480B. Solder resist layers 470 are formed on the interlayer resin insulating layers 541, respectively. Via holes 460 and conductor circuits 458 to be connected to the chip capacitors 420 are provided on the core substrate 430. The buildup wiring layers 480A and 480B are connected to each other by way of through holes 456 formed in the core substrate 430.

As shown in Fig. 30, each of the chip capacitors 420 consists of the first electrode 421, the second electrode 422 and a dielectric 423 put between the first and second electrodes. A plurality of pairs of first conductive films 424 connected to the first electrode 421 side and second conductive films 425 connected to the second electrode 422 side are arranged on the dielectric 423 to face one another.

As shown in Fig. 31, solder bumps 476U to be connected to the pads 492E, 492P and 492S of the IC chip 490 are provided on the upper buildup wiring layer 480A. Solder bumps 476D to be connected to the pads 494E1, 494E2, 494P1, 494P2 and 494S of the daughter board 495 are provided on the lower buildup wiring layer 480B.

The signal pad 492S of the IC chip 490 is connected to the signal pad 494S of the daughter board 495 through the bump 476U - the conductor circuit 559 - the via hole 564 - the conductor circuit 558 - the via hole 560 - the through hole 456 - the via hole 560 - the conductor circuit 558 - the via hole 564 - the conductor circuit 559 - the bump 476D.

The grounding pad 492E of the IC chip 490 is connected to the first electrodes 421 of the chip capacitors 420 through the bumps 476U - the via holes 564 - the conductor circuits 558 - the via holes 560 - the conductor circuits 458 - the via holes 460. The grounding pad 494E1 of the daughter board 495 is connected to the first electrodes 421 of the chip capacitors 420 through the bumps 476D - the via holes 564 - the conductor circuits 558 - the via holes 560 - the through holes 456 - the conductor circuits 458 - the via holes 460. The grounding pad 494E2 is connected to the first electrodes 421 of the chip capacitors 420 through the bumps 476D - the via holes 564 - the conductor circuits 558 - the via holes 560 - the conductor circuits 458 - the via holes 460.

The power supply pad 492P of the IC chip 490 is connected to the second electrodes 422 of the chip capacitors 420 through the bumps 476U - the via holes 564 - the conductor circuits 558 - the via holes 560 - the conductor circuits 458 - the via holes 460. The power supply pad 494P1 of the daughter board 495 is connected to the second electrodes 422 of the chip capacitors 420 through the bumps 476D - the via holes 564 - the conductor circuits 558 - the via holes 560 - the through holes 456 - the conductor circuits 458 - the via holes 460. The power supply pad 494P2 is connected to the first electrodes 422 of the chip capacitors 420 through the bumps 476D - the via holes 564 - the conductor circuits 558 - the via holes 560 - the conductor circuits 458 - the via holes 460. In this embodiment, the daughter board 495 side is connected to the first and second electrodes 421 and 422 of the chip capacitors 420 through the through holes 456. It is also possible to connect the daughter board 495 side thereto without employing the through holes.

As shown in Fig. 30, the core substrate 430 in this embodiment consists of the first resin substrate 430a to which

the chip capacitors 420 are connected through bonding materials, the second resin substrate 430b connected to the first resin substrate 430a through a bonding resin layer (bonding plate) 438a and the third resin substrate 430c connected to the second resin substrate 430b through a bonding resin layer (bonding plate) 438b. An opening 430B capable of containing the chip capacitors 420 are formed in the second resin substrate 430b.

With this structure, the chip capacitors 420 can be contained in the core substrate 430, so that the distance between the IC chip 490 and each chip capacitor 420 is shortened and the loop inductance of the printed circuit board 410 can be reduced. Further, the core substrate 430 is constituted by providing the first resin substrate 430a, the second resin substrate 430b and the third resin substrate 430c in a multilayer manner, the core substrate 430 can obtain sufficient strength. Moreover, since the core substrate 430 is constituted smoothly by providing the first resin substrate 430a and the third resin substrate 430c on the both sides of the core substrate 430, respectively, it is impossible to appropriately form the interlayer resin insulating layers 540, 541, the conductor circuits 558, 559 and the via holes 560 and 564 on the core substrate 430 and the probability of the occurrence of defective printed circuit boards can be decreased.

Furthermore, in this embodiment, the via holes 460 are provided on the both sides of the core substrate 430. This makes it possible to connect the daughter board 495 to each chip capacitors 420 at the shortest distance and high electric power can be supplied momentarily from the daughter board to the IC chip.

Moreover, in this embodiment, as shown in Fig. 25(D), an insulating bonding agent 436 is interposed between the first resin substrate 430a and each of the chip capacitors 420. Here,

the coefficient of the thermal expansion of the bonding agent 436 is set lower than that of the core substrate 430, i.e., set close to that of the chip capacitors 420 made of ceramic. Due to this, even if an internal stress resulting from the difference  
5 in the coefficient of thermal expansion among the core substrate, the bonding layers 436 and the chip capacitors 420, occurs in a heat cycle test, cracks, separation and the like less occur to the core substrate, making it possible to attain high reliability. It is also possible to prevent the occurrence of  
10 migration.

A method of manufacturing the printed circuit board described above with reference to Fig. 30 will be described with reference to Figs. 25 to 30.

(1) A one-sided copper-clad laminated plate 430M (first resin substrate 430a or the third resin substrate 430c) having a copper foil 432 laminated on one side of the resin substrate having a core having a thickness of 0.1 mm and made of glass cloth or the like which a BT (Bismaleimide-Triazine) resin is impregnated into and hardened in, is employed as a starting material (Fig.  
15 20 25(A)).

Next, the copper foil 432 of the copper-clad laminated plate 430M is etched into a pattern, thereby forming openings 432a for forming via holes are formed (Fig. 25(B)).

(2) Using a printer, a thermosetting or UV hardening bonding material 436 is applied onto portions of the first resin substrate 430a on which the copper foil 432 is not laminated (Fig. 25(C)). Instead of the application of the bonding material, potting may be performed.

Next, a plurality of chip capacitors 420 made of ceramic are mounted on the bonding material 436 and bonded to the first resin substrate 430a through the bonding material 436 (Fig.  
30 25(D)). Either one or a plurality of chip capacitors 420 may

be provided; however, if a plurality of chip capacitors 420 are employed, the high integration of the capacitors can be realized.

(3) Then, resin layers for bonding (bonding resin layers) 438a and 438b each having a core made of glass cloth or the like and impregnated with an epoxy resin as well as the second resin layer 430b (having a thickness of 0.4 mm) having a core made of glass cloth or the like which a BT resin is impregnated into and hardened in, are prepared. Openings 36A and 430B capable of containing the chip capacitors 420 are formed in the bonding resin layer 438a and the second resin layer 430b, respectively. First, the second resin substrate 430b is mounted on the third resin substrate 430c through the bonding resin layer 438b with the surface of the third resin substrate 430c laminated with the copper foil 432 directed downward. Next, the first resin substrate 430a is inverted and mounted on the second resin substrate 430b through the bonding resin layer 438a. Namely, the first resin substrate 430a is superposed on the second resin substrate 430b so that the chip capacitors 420 connected to the first resin substrate 430a are directed toward the bonding resin layer 438a side and can be contained in the opening 430B formed in the second resin substrate 430b (Fig. 26(A)). By doing so, the chip capacitors 420 can be contained in the core substrate 430 and the printed circuit board having reduced loop inductance can be provided.

It is noted that a substrate made of ceramic or AlN cannot be used as the core substrate. This is because such a substrate has poor workability for the outside shape thereof, sometimes cannot contain capacitors and has gaps even if filled with a resin.

(4) The superposed substrates are pressurized using a thermal press, thereby integrating the first, second and third resin substrates 430a, 430b and 430c in a multilayer manner and forming

the core substrate 430 having a plurality of chip capacitors 420 (Fig. 26(B)).

First, by pressurizing the substrates, the epoxy resin (insulating resin) is pushed outside of the bonding resin layers 438a and 438b and the gaps between the opening 430B and the chip capacitors 420 are filled with the resin. Further, since the substrates are pressurized and, at the same time, heated, the epoxy resin is hardened and the first resin substrate 430a, the second resin substrate 430b and the third resin substrate 430c are strongly bonded to one another by interposing the bonding resin layers 438a and 438b as bonding resin (bonding plates). In this embodiment, the space within the opening 430B is filled with the epoxy resin flowing out of the bonding resin layers. Alternatively, filler can be provided in the opening 430B.

Since the both sides of the core substrate 430 are the first resin substrate 430a and the third resin substrate 430c which are smooth, respectively, the interlayer resin insulating layers 540, 541, the conductor circuits 558, 559 and the via holes 560 and 564 can be appropriately formed in steps to be described later without damaging the smoothness of the core substrate 430 and the probability of the occurrence of defective printed circuit boards can be decreased. Further, the core substrate 430 can obtain sufficient strength.

(5) Next, the exposed regions of the copper foil 432 from the openings 432a for forming the via holes are removed by applying laser and openings 442 for via holes reaching the first and second electrodes 421 and 422 of the chip capacitors 420 are formed. Namely, using the copper foil 432 as a conformal mask, the openings 442 for via holes are formed in the core substrate 430 by applying laser. Then, the same step is executed to the other side of the substrate (Fig. 26(C)).

As a result, the opening diameters of the via holes depend

on the opening diameters of the openings 432a of the copper foil 432 for forming the via holes, thereby making it possible to form each via hole to have an appropriate diameter. Likewise, the positional accuracy of the via hole openings depend on the 5 opening positions of the openings 432a of the copper foil 432 for forming the via holes, thereby making it possible to form the via holes at appropriate positions even if the positional accuracy of the laser application is low.

(6) Penetrating holes 444 for through holes are formed in the 10 core substrate 430 by drilling or applying laser (Fig. 26(D)). Thereafter, a de-smear process is performed using oxygen plasma. Alternatively, a de-smear process using chemicals such as permanganate may be performed.

(7) Next, using SV-4540 manufactured by ULVAC JAPAN, Ltd., 15 a plasma process is performed to form rough surfaces on the entire surfaces of the core substrate 430. The plasma process is performed for two minutes while using, as inert gas, argon gas on conditions of power of 200 W, a gas pressure of 0.6 Pa and a temperature of 70°C. Then, sputtering is performed with Ni and Cu as targets and Ni-Cu metal layers 448 are formed on the 20 surfaces of the core substrate 430, respectively (Fig. 27(A)). While sputtering is employed herein, metal layers of copper, nickel or the like may be formed by electroless plating. In some cases, after performing sputtering, electroless plated 25 films may be formed. A roughing process may be performed using an acid or an oxidizer. The rough layers are preferably 0.1 to 5 µm thick.

(8) Next, photosensitive dry films are bonded onto the surfaces 30 of the Ni-Cu metal layers 448 and exposure and development processes are performed while mounting masks, thereby forming resists 450 each having a predetermined pattern. The core substrate 430 is then immersed in an electroplating solution,

current is applied to the substrate 430 through the Ni-Cu metal layers 448 and electroplating is conducted to portions in which the resists 450 are not formed on the following conditions, thereby forming electroplated films 452 (Fig. 27(B)).

5

[Electroplating Solution]

Sulfuric acid	2.24 mol/l
Copper sulfate	0.26 mol/l
Additive (Kaparacid HL)	19.5 mol/l

manufactured by Atotech Japan

[Electroplating Conditions]

Current density	1 A/dm <sup>2</sup>
Duration	120 minutes
Temperature	22±2°C

- 10 (9) After separating and removing the resists 450 with 5% NaOH, the Ni-Cu metal layers 448 and the copper foil 432 under the resists 450 are dissolved and removed by etching with an etching solution of a mixture of a nitride acid, a sulfuric acid and hydrogen peroxide, thereby forming conductor circuits 458  
15 (including via holes 460) and through holes 456 each consisting of the copper foil 432, the Ni-Cu metal layer 448 and the electroplated copper film 452. After washing and drying the resultant substrate, an etching solution is sprayed on the both sides of the substrate and the surfaces of the conductor circuits  
20 458 (including the via holes 460) and the through holes 456 are etched, thereby forming rough layers 462 on the entire surfaces of conductor circuits 458 (including the via holes 460) and the through holes 456 (Fig. 27(C)). As the etching solution, a mixture of 10 parts by weight of an imidazole copper (II) complex,  
25 7 parts by weight of an glycolic acid, 5 parts by weight of

DRAFT

potassium chloride and 78 parts by weight of ion-exchange water is employed.

(10) Resin filler 464 mainly consisting of an epoxy resin is applied on the both sides of the substrate 430 using the printer, thereby filling the resin filler 464 between the conductor circuits 458 and in the through holes 456, and heating and drying the resin filler 464. Namely, by executing this step, the resin filler 464 is filled between the conductor circuits 458 and in the via holes 460 and the through holes 456 (Fig. 25(D)).

(11) One side of the substrate 430 for which the process described in (10) above has been completed, is polished by belt sander polishing using belt abrasive paper (manufactured by Sankyo Rikagaku Co., Ltd.) in such a manner that the resin filler 464 is not left on the surfaces of the conductor circuits 458 and the land surfaces 456a of the through holes 456. Then, buffing is performed to remove flaws caused by the belt sander polishing. These series of polishing are also conducted to the other side of the substrate 430. Next, the resin filler 464 thus filled is heated and hardened. Thus, it is possible to obtain a wiring substrate wherein the surface layer portion of the resin filler 464 filled in the through holes 456 and the like and rough surfaces 462 on the upper surfaces of the conductor circuits 458 are removed, the both sides of the substrate 430 are smoothed, the resin filler 464 and the conductor circuits 458 are strongly bonded to one another through the rough surfaces 462, and the inner walls of the through holes 456 and the resin filler 464 are strongly bonded to one another through the rough surfaces 462.

Next, the same etching solution as that employed in (9) above is sprayed on the both sides of the substrate 430 to etch the surfaces of the conductor circuits 458 and the land surfaces 456a of the through holes 456 which have been flattened once,

thereby forming rough surfaces 458α on the entire surfaces of the conductor circuits 458 (Fig. 28(A)).

(12) Thermosetting epoxy resin sheets to be described later are laminated by vacuum pressing onto the substrate 430 which 5 has been subjected to the above-stated steps, at a pressure of 5 kg/cm<sup>2</sup> while raising temperature to 50 to 150°C, to thereby provide interlayer resin insulating layers 540 (Fig. 28(B)). The degree of vacuum during vacuum pressing is 10 mmHg.

(13) Next, openings 542 for via holes are formed in the 10 interlayer resin insulating layers 540 by applying laser (Fig. 28(C)).

(14) Using SV-4540 manufactured by ULVAC JAPAN, Ltd. employed in the step of (7), a plasma process is performed to form rough surfaces 540α on the surfaces of the interlayer resin insulating 15 layers 540 (Fig. 28(D)). Here, as in the case of the step of (7), a rouging process may be performed by using either an acid or an oxidizer. The rough layers are preferably 0.1 to 5 μm thick.

(15) Thereafter, as in the case of the step of (7), sputtering 20 is performed with Ni and Cu as targets, to thereby form Ni-Cu metal layers 548 on the surfaces of the interlayer resin insulating layers 540 (Fig. 29(A)). While sputtering is performed herein, metal layers of copper, nickel or the like may be formed by electroless plating. In some cases, after 25 forming the metal layers by sputtering, electroless plated films may be formed.

(16) Then, as in the case of the step of (8), photosensitive dry films are bonded onto the surfaces of the Ni-Cu metal layers 30 548 and exposure and development processes are performed while mounting masks, thereby forming resists 544 each having a predetermined pattern. The core substrate is then immersed in an electroplating solution, current is applied to the substrate

through the Ni-Cu metal layers 548 and electroplating is conducted to portions in which the resists 544 are not formed, thereby forming electroplated films 552 (Fig. 29(B)).

(17) Thereafter, the same process as in the step of (9) is 5 performed to thereby form conductor circuits 558 (including via holes 560) each consisting of the Ni-Cu metal layer 548 and the electroplated film 552. After washing and drying the resultant substrate, an etching solution is sprayed on the both sides of the substrate, which are thus etched, thereby forming rough 10 surfaces 154 on the entire surfaces of the conductor circuits 558 (including the via holes 560) (Fig. 29(C)).

(18) The steps of (12) to (17) are further repeated, thereby forming interlayer resin insulating layers 541, conductor 15 circuits 559 (including via holes 564) and rough surfaces 565 further above (Fig. 29(D)).

Later steps are the same as those of (16) to (19) in the first embodiment stated above, which description will not be, therefore, given herein.

The mounting of the IC chip 490 on the printed circuit 20 board 410 completed through the above steps and the attachment of the printed circuit board 410 to the daughter board 495 are the same as those in the first embodiment, which description will not be, therefore, given herein.

25 [First Other Example of Third Embodiment]

A printed circuit board according to the first other example of the third embodiment of the present invention will be described hereinafter with reference to Fig. 32. The printed circuit board in the first other example is almost the same as 30 the printed circuit board in the third embodiment stated above. However, in the printed circuit board in the first other example, conductive connection pins 496 are provided at the printed

circuit board and the printed circuit is connected to a daughter board through the conductive connection pins 496.

Further, in the third embodiment stated above, only the chip capacitors 420 contained in the core substrate 430 are 5 provided. In this example, mass storage chip capacitors 486 are mounted on the front and reverse sides of the substrate.

The IC chip momentarily consumes high power and performs complex arithmetic operation. In the first other example, to supply high power to the IC chip, chip capacitors 420 and chip 10 capacitors 486 for power supply are provided. The advantage derived from these chip capacitors will be described with reference to Fig. 12.

Fig. 12 is a graph with a vertical axis indicating voltage supplied to the IC chip and a horizontal axis indicating time.

15 In Fig. 12, two-dot chain line C denotes the voltage variation of a printed circuit board which is not provided with power supply capacitors. If power supply capacitors are not provided, voltage attenuates greatly. A broken line A denotes the voltage variation of a printed circuit board having chip capacitors 20 mounted on the surfaces thereof. Compared with the two-dot chain line C, voltage does not drop greatly. However, since loop length is larger, rate-controlled power supply cannot be conducted sufficiently. Namely, at the start of the supply of power, voltage falls. Further, a two-dot chain line B denotes the voltage 25 variation of a printed circuit board including the chip capacitors described above with reference to Fig. 31. In this case, loop length can be shortened; however, mass storage chip capacitors cannot be contained in a core substrate 430 and voltage, therefore, varies. Here, a solid line E denotes the voltage 30 variation of the printed circuit board in the first other example which printed circuit board has the chip capacitors 420 mounted in the core substrate and the mass storage chip capacitors 486

mounted on the surfaces thereof. Voltage variation is minimized by providing the chip capacitors 420 and the mass storage chip capacitors 486 (having relatively high inductance) in the vicinity of the IC chip.

5

[First Modification of Third Embodiment]

Next, a printed circuit board 414 according to the first modification of the third embodiment will be described with reference to Fig. 36. The printed circuit board in the first 10 modification of the third embodiment is almost the same in constitution as the printed circuit board in the third embodiment stated above. In the third embodiment described above with reference to Fig. 30, each conductor circuit 458 consists of three layers, i.e., the copper foil 432, the Ni-Cu metal layer 15 448 and the electroplated film 452. In the printed circuit board 414 in the first modification of the third embodiment, by contrast, each conductor circuit 458 consists of two layers, i.e., an electroless plated film 443 and an electroplated film 452. Namely, the copper foil 432 is removed and thickness is reduced, 20 thereby forming the conductor circuit 458 at fine pitch.

In addition, in the printed circuit board 414 in the first modification of the third embodiment, conductor circuits 435 are formed on the both sides of the second resin substrate 430b provided with an opening 430B for containing chip capacitors 25 420. In the first modification of the third embodiment, since the conductor circuits 435 are formed on the both sides of the second resin substrate 430b provided with the opening 430B for containing the chip capacitors 420, it is possible to increase wiring density within the core substrate 430 and to reduce the 30 number of interlayer resin insulating layers to be built up.

Furthermore, as shown in Fig. 13(A), in the chip capacitor 420 of the printed circuit board in the first modification of

the third embodiment, after the coating layer (not shown) of the first and second electrodes 421 and 422 are completely separated, the first and second electrodes 421 and 422 are coated with copper plated films 29. The first and second electrodes 5 421 and 422 each coated with the copper plated film 29 are electrically connected to each other by via holes 460 made of a copper plated material. Here, the electrodes 421 and 422 of the chip capacitor are made by metalization and have irregular portions on the surfaces thereof. Due to this, if the substrate 10 is used while exposing the metal layers, the resin may sometimes remain on the irregular portions in the step of providing non-penetrating holes 442 in the first resin substrate 430a. At this time, the resin residue causes connection defects between the first, second electrodes 421, 422 and the via holes 460. 15 In the first modification of the third embodiment, by contrast, since the surfaces of the first and second electrodes 421 and 422 are smoothed by the copper plated films 29, no resin remains when providing openings 442 in the coated first resin substrate 430a on the electrodes and the reliability of the connection 20 between the electrodes 421, 422 and the via holes 460 when forming the via holes 460 can be enhanced.

Furthermore, the via holes 460 are formed by plating in the electrodes 421 and 422 having the copper plated films 29 formed thereon, respectively, the connection characteristic 25 between the electrodes 421, 422 and the via holes 460 is good and disconnection does not occur between the electrodes 421, 422 and the via holes 460 even if a heat cycle test is conducted. Besides, no migration occurs and no disadvantages are derived in the connection section of the via holes of the capacitors.

30 The copper plated films 29 are provided after the nickel / tin layer (coating layer) coated on the surface of each metal layer 26 in a phase of manufacturing chip capacitors is separated

in a phase of mounting the chip capacitors on the printed circuit board. Alternatively, the copperplated films 29 can be directly coated on the metal layers 26 in the phase of manufacturing the chip capacitors 420. Namely, in the first modification of the  
5 third embodiment, as in the case of the third embodiment, after openings reaching the copper plated films 29 of the electrodes are provided by applying laser, a de-smear process is performed to thereby form via holes by copper plating. Accordingly, even if an oxide film is formed on the surface of the copper plated  
10 film 29, the oxide film can be removed by the laser and de-smear processes, thereby making it possible to establish connection appropriately.

Further, rough layers 23a are provided on the surfaces of a dielectric 423 of each chip capacitor 420 which dielectric is made of ceramic. Due to this, the adhesiveness between the chip capacitors 420 made of ceramic and the resin substrates 438a and 438b made of a resin is high and the first resin substrate 430a is not separated on the interface therebetween even if a heat cycle test is conducted. The rough layers 23a can be formed  
15 by polishing the surfaces of the chip capacitors 420 after sintering them or by roughing the surfaces before sintering them.  
20 In the first modification of the third embodiment, the surfaces of the capacitors are roughed and the adhesiveness between the capacitors and the resin is thereby enhanced. Alternatively,  
25 a silane coupling process can be conducted to the surfaces of the capacitors.

As shown in Fig. 13(B), it is also possible to employ the first and second electrodes 21 and 22 of the capacitors 420 while removing part of the coats 28 of the electrodes 21 and 22. This  
30 is because connection characteristics can be enhanced by exposing the first and second electrodes 21 and 22.

A process for manufacturing the printed circuit board

according to the first modification of the third embodiment of the present invention will be described with reference to Figs. 33 to 35.

(1) One-sided copper-clad laminated plates 430M (the first resin substrate 430a and the third resin substrate 430c) each having a copper foil 432 laminated on one side of a resin substrate having a core having a thickness of 0.1 mm and made of glass cloth or the like which a BT (Bismaleimide-Triazine) resin is impregnated into and hardened in, is prepared. Also, a two-sided copper-clad laminated plate 430N (the second resin substrate 430b) having a copper foil 432 laminated on the both sides of a resin substrate having a core having a thickness of 0.4 mm and made of glass cloth or the like which a BT (Bismaleimide-Triazine) resin is impregnated into and hardened in, is prepared (Fig. 33(A)).

(2) Next, the copper foil 432 of each copper-clad laminated plate 430M is etched into a pattern, thereby forming openings 432a for forming via holes are formed. Likewise, the copper foils 432 of the both-sided copper-clad laminated plate 430N are etched into a pattern, thereby forming conductor circuits 435 (Fig. 33(B)). In the first modification of the third embodiment, the conductor circuit 435 are formed on the both sides of the second resin substrate 430b, so that the wiring density of the core substrate can be advantageously increased and that the number of interlayer resin insulating layers to be built up can be advantageously reduce.

(3) Using a printer, a thermosetting or UV hardening bonding material 436 is applied onto portions of the first resin substrate 430a on which the copper foils 432 are not laminated (Fig. 33(C)). Instead of the application of the bonding material, potting may be performed.

Next, a plurality of chip capacitors 420 made of ceramic

are mounted on the bonding material 436 and bonded to the first resin substrate 430a through the bonding material 436 (Fig. 33(D)). Either one or a plurality of chip capacitors 420 may be provided; however, if a plurality of chip capacitors 420 are employed, the high integration of the capacitors can be realized.

(4) Then, resin layers for bonding (bonding resin layers) 438a and 438b each having a core made of glass cloth or the like and impregnated with an epoxy resin as well as the second resin layer 430b are prepared. Openings 36A and 430B capable of containing the chip capacitors 420 are formed in the bonding resin layer 438a and the second resin layer 430b, respectively. First, the second resin substrate 430b is mounted on the third resin substrate 430c through the bonding resin layer 438b with the surface of the third resin substrate 430c laminated with the copper foil 432 directed downward. Next, the first resin substrate 430a is inverted and mounted on the second resin substrate 430b through the bonding resin layer 438a. Namely, the first resin substrate 430a is superposed on the second resin substrate 430b so that the chip capacitors 420 can be contained in the opening 430B formed in the second resin substrate 430b (Fig. 34(A)). By doing so, the chip capacitors 420 can be contained in the core substrate 430 and the printed circuit board having reduced loop inductance can be provided.

(5) The superposed substrates are pressurized using a thermal press, thereby integrating the first, second and third resin substrates 430a, 430b and 430c in a multilayer manner and forming the core substrate 430 having a plurality of chip capacitors 420 (Fig. 34(B)).

In this embodiment, the epoxy resin flowing out of the bonding resin layers is filled in gaps within the openings 430. Alternatively, filler may be arranged in the openings 430B.

Since the both sides of the core substrate 430 are the

first resin substrate 430a and the third resin substrate 430c which are smooth, respectively, the interlayer resin insulating layers 540, 541, the conductor circuits 558, 559 and the via holes 560 and 564 can be appropriately formed in steps to be described later without damaging the smoothness of the core substrate 430 and the probability of the occurrence of defective printed circuit boards can be decreased. Further, the core substrate 430 can obtain sufficient strength.

(6) Next, the exposed regions of the copper foils 432 from the openings 432a for forming the via holes are removed by applying laser and openings 442 for via holes reaching the first and second electrodes 421 and 422 of the chip capacitors 420 are formed. Namely, using the copper foils 432 as conformal masks, the openings 442 for the via holes are formed in the core substrate 430. Then, the same step is executed to the other side of the substrate (Fig. 34(C)). As a result, the opening diameters of the via holes depend on the opening diameters of the openings 432a of the copper foils 432 for forming the via holes, thereby making it possible to form each via hole to have an appropriate diameter. Likewise, the positional accuracy of the via hole openings depend on the opening positions of the openings 432a of the copper foil 432 for forming the via holes, thereby making it possible to form the via holes at appropriate positions even if the positional accuracy of the laser application is low.

(7) Thereafter, the copper foils 432 on the both sides of the core substrate 430 are etched by using an etching solution and thereby removed. By doing so, it is possible to form the thinner conductor circuits 458 in the later step to be described later and form the circuits 458 at fine pitch.

Next, penetrating holes 444 for through holes are formed in the core substrate 430 by drilling or applying laser (Fig. 34(D)). Thereafter, a de-smear process is performed using

oxygen plasma. Alternatively, a de-smear process using chemicals such as permanganate may be performed.

(8) Next, using SV-4540 manufactured by ULVAC JAPAN, Ltd., a plasma process is performed to form rough surfaces 446 on the 5 entire surfaces of the core substrate 430 (Fig. 35(A)). The plasma process is performed for two minutes while using, as inert gas, argon gas on conditions of power of 200 W, a gas pressure of 0.6 Pa and a temperature of 70°C. Alternatively, a roughing process may be performed using an acid or an oxidizer. The rough 10 layers are preferably 0.1 to 5 µm thick.

(9) Next, the substrate 430 is immersed in an electroless copper plating solution having the following composition to thereby form electroless copper plated films 443 each having a thickness of 0.6 to 3.0 µm on the entirety of the rough surfaces 15 446 (Fig. 35(B)).

#### [Electroless Plating Solution]

NiSO <sub>4</sub>	0.003 mol/l
tartaric acid	0.200 mol/l
copper sulfate	0.043 mol/l
HCHO	0.050 mol/l
NaOH	0.100 mol/l
α,α'-bipyridyl	40 mg/l
Polyethylene glycol (PEG)	0.10 g/l

#### [Electroless Plating Conditions]

20 40 minutes at a solution temperature of 35°C.

While electroless plating is employed in this embodiment, metal layers of copper, nickel or the like may be formed by sputtering. In some cases, after forming the layers by 25 sputtering, electroless plated films may be formed.

(10) Commercially available photosensitive dry films are bonded onto the electroless copper plated films 443. Masks are mounted on the films, respectively and the films are exposed with 100 mJ/cm<sup>3</sup> and developed with a 0.8% sodium carbonate solution, thereby providing plating resists 450 each having a thickness of 30 µm. Then, the substrate 430 is washed with water of a temperature of 50°C and degreased, washed with water of a temperature of 25°C and with a sulfuric acid, and subjected to copper electroplating on the following conditions, thereby forming electroplated copper films 452 each having a thickness of 20 µm (Fig. 35(C)).

[Electroplating Solution]

Sulfuric acid	2.24 mol/l
Copper sulfate	0.26 mol/l
Additive	19.5 mol/l

(Kaparacid HL manufactured by Atotech Japan)

[Electroplating Conditions]

Current density	1 A/dm <sup>2</sup>
Duration	65 minutes
temperature	22±2°C

(11) After separating and removing the resists 450 with 5% NaOH, the electroless plated films 443 under the resists 450 are dissolved and removed by etching with an etching solution of a mixture of a sulfuric acid and hydrogen peroxide, thereby forming conductor circuits 458 (including via holes 460) and through holes 456 each consisting of the electroless copper plated film 443 and the electroplated copper film 452 each having a thickness of 18 µm (Fig. 35(D)). In the first modification of the third embodiment, the copper foils 432 are removed in

advance as stated above, whereby the conductor films 458 can made thinner and formed at fine pitch. While the copper foils 432 are completely separated in this modification, it is also possible to make the conductor circuits 458 thinner and form 5 the conductor circuits 458 at fine pitch by making the copper foils 432 thinner by light etching.

Later steps are the same as those of (10) to (18) in the third embodiment stated above, which description will not be, therefore, given herein.

10 In the first modification of the third embodiment stated above, the via holes are provided on the both sides of the core substrate. It is also possible to form via holes only on one side of the substrate. Further, the openings 432a of the copper foils 432 on the surfaces of the core substrate 430 are employed 15 as conformal masks in this modification. It is also possible to provide openings reaching the capacitors by applying laser without employing the conformal masks of the core substrate 430.

20 [Second Modification of Third Embodiment]

Next, the constitution of a printed circuit board according to the second modification of the first embodiment will be described with reference to Fig. 14.

The printed circuit board in the second modification is almost the same in constitution as the printed circuit board 25 in the first embodiment stated above. They, however, differ in chip capacitors 20 contained in the core substrate 30. Fig. 14 is a plan view of chip capacitors. Fig. 14(A) shows a chip capacitor before being cut for providing a plurality of chip capacitors. In Fig. 14(A), a dashed line denotes a cut line. 30 As shown in Fig. 14(B), in the printed circuit board in the first embodiment stated above, the first electrodes 21 and the second electrodes 22 are provided on the edges of the chip capacitor.

Fig. 14(C) shows a chip capacitor before being cut for providing a plurality of chip capacitors in the second modification. In Fig. 14(C), a dashed line denotes a cut line. In the printed circuit board in the second modification, as shown in the plan view of Fig. 14(D), first electrodes 21 and second electrodes 22 are provided inside of the edges of the chip capacitor.

In the printed circuit board in the second modification, the chip capacitors 20 each having electrodes formed inside of the outer edges thereof are employed, so that mass storage chip capacitors can be employed.

Next, a printed circuit board according to the first other example of the second modification will be described with reference to Fig. 15.

Fig. 15 is a plan view of a chip capacitor 20 contained in the core substrate of the printed circuit board according to the first other example. In the first embodiment stated above, a plurality of small storage chip capacitors are contained in the core substrate. In the first other example, by contrast, a large, mass storage chip capacitor 20 is contained in the core substrate. The chip capacitor 20 consists of the first electrodes 21, the second electrodes 22, a dielectric 23, the first conductive films 24 connected to the first electrodes 21, the second conductive films 25 connected to the second electrodes 22, electrodes 27 which are not connected to the first and second conductive films 24 and 25, for the connection of the upper and lower surfaces of the chip capacitor. The IC chip and the daughterboard are connected to each other through the electrodes 27.

Since the large chip capacitor is employed in the printed circuit board in the first modification, it is possible to employ a mass storage chip capacitor. Further, since the large chip capacitor 20 is employed, the printed circuit board does not

warp even if a heat cycle is performed repeatedly.

Next, a printed circuit board according to the second other example of the second modification will be described with reference to Fig. 16. Fig. 16(A) shows a chip capacitor before being cut for providing a plurality of chip capacitors. In Fig. 16(A), a dashed line denotes an ordinary cut line. Fig. 16(B) is a plan view of the chip capacitors. As shown in Fig. 16(B), a plurality of (or in Fig. 16(B), three) chip capacitors for providing multiple capacitors are coupled to one another and employed as a large capacitor as a whole.

In the second other example, since the large chip capacitor 20 is employed, it is possible to employ a mass storage chip capacitor. Further, since the large chip capacitor 20 is employed, the printed circuit board does not warp even if a heat cycle is performed repeatedly.

In the embodiment stated above, the chip capacitors are built in the printed circuit board. Alternatively, plate-like capacitors each constituted by providing a conductive film on a ceramic plate may be employed instead of the chip capacitors.

The structure of the third embodiment makes it possible to contain the capacitors in the core substrate and to shorten the distance between the IC chip and each capacitor, thereby reducing the loop inductance of the printed circuit board. Further, since the printed circuit board is constituted by providing resin substrates in a multilayer manner, the core substrate can obtain sufficient strength. Besides, the first resin substrate and the third resin substrate are provided on the both sides of the core substrate, respectively, thereby constituting the core substrate smoothly. Thus, it is possible to appropriately form interlayer resin insulating layers and conductor circuits on the core substrate and to thereby decrease the probability of the occurrence of defective printed circuit

boards.

In addition, by adopting the manufacturing method of the third embodiment, the opening diameters of the via holes depend on the opening diameters of the openings of metal films, so that  
5 it is possible to form each via hole to have an appropriate diameter. Likewise, the positional accuracy of the via hole openings depend on the opening positions of the openings of the metal films, so that it is possible to form the via holes at appropriate positions even if the positional accuracy of the laser  
10 application is low.

Since it is possible to connect the substrate from the lower portions of the capacitors, the structure allows reducing the loop inductance and increasing the degree of freedom for arrangement.

15 Moreover, since the resin is filled between the core substrate and the capacitors, a stress resulting from the capacitors or the like can be reduced even if it occurs and no migration occurs. Due to this, there is no fear that the electrodes of the capacitors are separated from the connection sections of the via holes and dissolved. Thus, it is possible to maintain desired performance even if a reliability test is  
20 executed.

In addition, even if the capacitors are coated with copper, it is possible to prevent the occurrence of migration.

25

#### [Fourth Embodiment]

A printed circuit board according to the fourth embodiment of the present invention will be described hereinafter with reference to Figs. 42 to 44. Fig. 42 is a cross-sectional view  
30 of a printed circuit board 610. Fig. 43 shows a state in which an IC chip 690 is mounted on the printed circuit board 610 shown in Fig. 42 and that the printed circuit board 610 is attached

to a daughter board 694. Fig. 44(A) is an enlarged view of a via hole 660 shown in Fig. 42. Fig. 44(B) is a typical view showing a state in which a plurality of via holes 760 are provided in the via hole 660 shown in Fig. 44(A), which view is seen from 5 an arrow B side.

As shown in Fig. 42, the printed circuit board 610 consists of a core substrate 630 containing a plurality of chip capacitors 620, and buildup wiring layers 680A and 680B. Relatively large via holes 660 are connected to the electrodes 621 and 622 of 10 the plural chip capacitors 620 contained in the core substrate 630. Each of the buildup wiring layers 680A and 680B consists of interlayer resin insulating layers 740 and 741. Conductor circuits 758 and relatively small via holes 760 are formed on 15 the interlayer resin insulating layers 740, whereas conductor circuits 759 and relatively small via holes 764 are formed on the interlayer resin insulating layers 741. Solder resist layers 670 are provided on the interlayer resin insulating layers 741, respectively.

As shown in Fig. 13(A), each of the chip capacitors 620 consists of the first electrode 621, the second electrode 622 and a dielectric 23 put between the first and second electrodes. A plurality of pairs of the first conductive films 24 connected 20 to the first electrode 621 side and the second conductive films 25 connected to the second electrode 622 side are arranged on the dielectric 23 to face one another. It is noted that as shown 25 in Fig. 13(B), part of coats 28 of the first electrodes 21 and the second electrodes 22 of the capacitors 620 can be removed. This is because the connection characteristics with respect to 30 the via holes made by plating can be enhanced by exposing the first and second electrodes 21 and 22.

As shown in Fig. 43, solder bumps 676U to be connected to the pads 692 of the IC chip 690 are formed on the via hole

764 of the upper buildup wiring layer 680A. Solder bumps 676D to be connected to the pads 694 of the daughter board 695 are formed on the via holes 764 of the lower buildup wiring layer 680B.

5 A resin substrate is employed as the core substrate. For example, a resin material used for an ordinary printed circuit board such as a glass epoxy resin impregnated material, a phenol resin impregnated material or the like can be employed. However, substrates made of ceramic or AlN cannot be employed as the core  
10 substrate. This is because such a substrate has poor workability for the outside shape thereof, sometimes cannot contain capacitors and has gaps even if filled with a resin.

15 Also, a plurality of chip capacitors 620 are contained in a concave portion 734 formed in the core substrate, so that it is possible to arrange the chip capacitors 620 with high density. Further, since a plurality of chip capacitors 620 are contained in the concave portion 734, it is possible to make the heights of the chip capacitors 620 uniform. Due to this, the thicknesses  
20 of the resin layers 640 on the chip capacitors 620 can be made uniform, so that it is possible to appropriately form via holes 660. Besides, since the distance between the IC chip 690 and each chip capacitor 620 becomes shorter, so that it is possible to reduce loop inductance.

25 In addition, as shown in Fig. 44(A) which is an enlarged view of the via hole 660 shown in Figs. 42 and 43, a plurality of via holes 760 in the upper buildup wiring layer 680A are connected to one via hole 660. The large via hole 660 as shown in Fig. 44(B) is formed to have an inside diameter of 125  $\mu\text{m}$  and a land diameter of 165  $\mu\text{m}$ , the small via hole 760 is formed  
30 to have an inside diameter of 25  $\mu\text{m}$  and a land diameter of 65  $\mu\text{m}$ . On the other hand, the chip capacitors 620 are formed rectangularly and the first and the second electrode 621 and the

C  
O  
P  
Y  
R  
I  
G  
H  
T  
S  
P  
A  
C  
E

second electrode 621 of each capacitor are formed rectangularly to have one side of 250  $\mu\text{m}$ . Due to this, even if the positions at which the chip capacitors are arranged are shifted by several tens of  $\mu\text{m}$ , it is possible to establish connection between the 5 first electrodes 621 and the second electrodes 622 of the chip capacitors 620 and the via holes 660, thereby ensuring the supply of power from the chip capacitors 620 to the IC chip 690. Further, by providing a plurality of via holes 760, the same effect as that of connecting inductances in parallel. Due to this, the 10 high frequency characteristics of power supply lines and ground lines are enhanced, thereby making it possible to prevent the malfunction of the IC chip due to lack of supply of power or the variation of earth level. Moreover, since the wiring length to each chip capacitor 620 from the IC chip can be shortened, 15 it is possible to reduce loop inductance.

As shown in Fig. 42, the via holes 660 are formed as filled via holes filled with a plated material and having flat surfaces. This makes it possible to directly connect a plurality of via holes 760 onto the via hole 660. Thus, it is possible to enhance the characteristics of the connection between the via holes 660 and 760 and to ensure the supply of power from the chip capacitors 620 to the IC chip 690. In this embodiment, the filled via holes are formed by filling a plated material within the holes. It is also possible to employ filled via holes each having a metal film provided on the front surface after filling a resin in the 20 holes. 25

The coefficients of thermal expansion of resin filler 633 and a bonding material 636 below the chip capacitors 620 are set lower than those of the core substrate 630 and resin insulating 30 layers 640, i.e., set close to those of the chip capacitors 620 made of ceramic. Due to this, even if an internal stress resulting from difference in the coefficient of thermal expansion

occurs among the core substrate 630, the resin insulating layers 640 and the chip capacitors 620 during a heat cycle test, cracks, separation and the like less occurs to the core substrate 630 and the resin insulating layers 640, thereby making it possible  
5 to attain high reliability.

Furthermore, since through holes 656 are formed in the resin layers 633 between the chip capacitors 620, no signal lines pass through the chip capacitors 620 made of ceramic. Thus,  
10 propagation delay caused by reflection due to the discontinuous impedance by a high dielectric and the passage of the high dielectric does not occur.

As shown in Fig. 13(A), in the chip capacitor 620, a copper plated film 29 is coated on the surface of a metal layer 26 constituting the first electrode 621 and the second electrode  
15 622. The plated film coat is formed by plating such as electroplating and electroless plating. As shown in Fig. 42, the first and second electrodes 621 and 622 coated with the copper plated films 29 are electrically connected to the via holes 660 made of a copper plated material. Here, the electrodes 621 and  
20 622 of the chip capacitors are formed by metalization and have irregular portions on the surfaces thereof. Due to this, if the substrate is used while exposing the metal layers 26, resin may sometimes remain on the irregular portions in a step of providing openings 639 in resin insulating layers 640 as will  
25 be described later. At this time, the resin residue causes connection defects between the first, second electrodes 621 and 622 and the via holes 660. To prevent this, the surfaces of the first and second electrodes 621 and 622 are smoothed by the copper plated films 29. Thus, no resin remains when providing  
30 the openings 639 in the resin insulating layers 640 coated on the electrodes and the reliability of the connection between the electrodes 621, 622 and the via holes 660 when forming the

via holes 660 can be enhanced.

Furthermore, since the via holes 660 are formed by plating in the electrodes 621 and 622 having the copper plated films 29 formed thereon, respectively, the characteristic of the 5 connection between the electrodes 621, 622 and the via holes 660 is high and disconnection does not occur between the electrodes 621, 622 and the via holes 660 even if a heat cycle test is conducted.

The copper plated films 29 are provided after the nickel / tin layer (coating layer) coated on the surface of each metal layer 26 in a phase of manufacturing chip capacitors is separated in a phase of mounting the chip capacitors on the printed circuit board. Alternatively, the copper plated films 29 can be directly coated on the metal layers 26 in the phase of manufacturing the 15 chip capacitors 220. Namely, in this embodiment, after openings reaching the copper plated films 29 of the electrodes are provided by applying laser, a de-smear process is performed to thereby form via holes by copper plating. Accordingly, even if an oxide film is formed on the surface of the copper plated film 29, the 20 oxide film can be removed by the laser and de-smear processes, thereby making it possible to establish connection appropriately.

Further, rough layers 23 $\alpha$  may be provided on the surfaces of the dielectrics 23 of the chip capacitors 620 which dielectrics are made of ceramic. By doing so, the adhesiveness between the chip capacitors 620 made of ceramic and the interlayer resin insulating layer 640 made of a resin is high and the interlayer resin insulating layer 640 is not separated on the interface therebetween even if a heat cycle test is conducted. The rough 25 layers 23 $\alpha$  can be formed by polishing the surfaces of the chip capacitors 620 after sintering them or by roughing the surfaces 30 before sintering them. In this embodiment, the surfaces of the

capacitors are roughed and the adhesiveness between each capacitor and the resin is thereby enhanced. Alternatively, a silane coupling process can be conducted to the surfaces of the capacitors.

5 Next, a method of manufacturing the printed circuit board described above with reference to Fig. 42 will be described with reference to Figs. 37 to 42.

(1) First, a core substrate 630 consisting of an insulating resin substrate is employed as starting material (Fig. 37(A)).

10 Next, a concave portion 734 for providing capacitors therein is formed on one side of the core substrate 630 by conducting spot facing or by providing a through hole in the insulating resin, followed by pressing and bonding (Fig. 37(B)). The concave portion 734 is formed to be wider than an area in which 15 a plurality of capacitors can be arranged. By doing so, it is possible to ensure that a plurality of capacitors are provided in the core substrate 630.

(2) Then, using a printer, a bonding material 636 is applied onto the concave portion 734 (Fig. 37(C)). Alternatively, the bonding material can be applied onto the concave portion by a potting, a die-bonding method, a method of applying a bonding sheet or the like. As the bonding material 636, one having a lower coefficient of expansion than that of the core substrate is employed. Next, a plurality of chip capacitors 620 made of 25 ceramic are bonded to the concave portion 734 through the bonding material 636 (Fig. 37(D)). Here, by providing a plurality of capacitors 620 in the concave portion 734 having a flat base, the heights of the plural chip capacitors 620 are made uniform. Therefore, it is possible to form interlayer resin insulating 30 layers 640 on the core substrate 630 to have uniform thickness and to appropriately form via holes 660 in later steps.

Then, the upper surfaces of the plural chip capacitors

620 are pressed or struck to thereby make the heights of the capacitors 620 uniform (Fig. 37(E)). Through this step, in providing a plurality of chip capacitors 620 within the concave portion 734, the heights of the chip capacitors 620 can be made  
5 completely uniform and the core substrate 630 can be made smooth even if the sizes of the plural chip capacitors 620 are uneven.

(3) Thereafter, a thermosetting resin is filled between the chip capacitors 620 within the concave portion 734, heated and hardened to thereby form an interlayer rein insulating layer  
10 633 (Fig. 38(A)). As the thermosetting resin, an epoxy resin, a phenol resin, a polyimide resin or a triazine resin is preferable. As a result, the chip capacitors 620 within the concave portion 734 can be fixed. The resin layer 633 having a lower coefficient of thermal expansion than that of the core substrate is employed.  
15

Alternatively, a thermoplastic resin may be employed. It is also possible to impregnate filler in a resin so as to match the coefficient of thermal expansion. The filler involves, for example, inorganic filler, ceramic filler, metal filler and the like.

(4) Further, using the printer, an epoxy resin or a polyolefin resin is applied on the resultant substrate to thereby form a resin insulating layer 640 (Fig. 38(B)). Instead of applying a resin, a resin film may be bonded.

Alternatively, one type or more of a thermosetting resin,  
25 a thermoplastic resin, a complex of a photosensitive resin, a thermosetting resin and a thermoplastic resin, a complex of a photosensitive resin and a thermoplastic resin and the like can be employed. Two layers may be constituted using them.

(5) Next, openings 639 for relatively large via holes are  
30 formed in the resin insulating layer 640 by applying laser (Fig. 38(C)). A de-smear process follows. Instead of applying laser, exposure and development processes can be performed. Holes 644

for through holes are formed in the resin layer 633 by drilling or applying laser, heated and hardened (Fig. 38(D)). In some cases, a roughing process using an acid or an oxidizer or a roughing process by a plasma process may be performed. By doing so, the adhesiveness of the rough layers is ensured.

(6) Thereafter, a copper plated film 729 is formed on the surface of the resin insulating layer 640 by electroless copper plating (Fig. 39(A)). Instead of electroless plating, sputtering may be conducted with Ni and Cu as targets to form an Ni-Cu metal layer. Alternatively, after forming the metal layer by sputtering, an electroless plated film may be formed.

(7) Next, photosensitive dry films are bonded onto the surfaces of the copper plated films 729, exposed and developed while mounting masks, thereby forming resists 649 each having a predetermined pattern. The core substrate 630 is immersed in an electroplating solution, current is applied through the copper plated films 729 and electroplated plates 651 are formed on portions on which the resists 649 are not formed (Fig. 39(B)).

(8) After separating and removing the plating resists 649 with 5% NaOH, the copper plated films 729 under the plating resists 649 are etched, dissolved and removed by a solution mixture of a sulfuric acid and hydrogen peroxide, thereby forming relative large via holes 660 and through holes 656 each having a filled via hole structure consisting of the copper plated film 729 and the electroplated copper film 651. The diameters of the large via holes are preferably within a range of 100 to 600  $\mu\text{m}$ . The diameters are more preferably 125 to 350  $\mu\text{m}$ . In this case, the large via holes are each formed to have a diameter of 165  $\mu\text{m}$ . The through holes are each formed to have a diameter of 250  $\mu\text{m}$ . An etching solution is sprayed on the both sides of the substrate 630 to etch the surfaces of the via holes 660 and the land surfaces of the through holes 656, thereby forming rough

surfaces 660α on the entire surfaces of the via holes 660 and the through holes 656 (Fig. 39(C)).

(9) Thereafter, resin filler 664 mainly consisting of an epoxy resin is filled in the through holes 656, and dried (Fig. 39(D)).

5 (10) Thermosetting epoxy resin sheets each having a thickness of 50 μm are laminated by vacuum pressing on the both sides of the substrate 630 which has been subjected to the above-stated steps, respectively, at a pressure of 5 kg/cm<sup>2</sup> while raising temperature to 50 to 150°C to thereby provide interlayer resin  
10 insulating layers 740 made of an epoxy resin (Fig. 40(A)). The degree of vacuum during vacuum pressing is 10 mmHg. A cycloolefin resin instead of the epoxy resin can be employed.

15 (11) Next, openings 642 for relatively small via holes are formed in the interlayer resin insulating layers 740 having a thickness of 65 μm by applying CO<sub>2</sub> gas laser (Fig. 40(B)). The diameters of the relatively small via holes are preferable in a range of 25 to 100 μm. Then, a de-smear process is performed using oxygen plasma.

20 (12) Next, using SV-4540 manufactured by ULVAC JAPAN, Ltd., a plasma process is performed to rough the surfaces of the interlayer resin insulating layers 740, thereby forming rough surfaces 646 (Fig. 40(C)). The plasma process is performed for two minutes while using, as inert gas, argon gas on conditions of power of 200 W, a gas pressure of 0.6 Pa and a temperature  
25 of 70°C. The roughing process may be performed using either an acid or an oxidizer. The rough layers are preferably 0.1 to 5 μm.

30 (13) Next, after exchanging argon gas contained inside, using the same device, sputtering is performed on conditions of an atmospheric pressure of 0.6 Pa, a temperature 80 °C, power of 200 W and a duration of 5 minutes with Ni and Cu as targets and Ni-Cumetal layers 648 are formed on the surfaces of the interlayer

resin insulating layers 740, respectively. At this time, the thickness of each of the formed Ni-Cu metal layers 648 is 0.2  $\mu\text{m}$  (Fig. 40(D)). Plated films such as electroless plated films may be formed or plated films may be formed on the sputtered

5 surfaces.

(14) Commercially available photosensitive dry films are bonded onto the both sides of the substrate 630 for which the above processes have been completed, photomask films are mounted thereon, the films are exposed with  $100 \text{ mJ/cm}^2$  and then developed

10 with a 0.8% sodium carbonate solution, thereby providing plating resists 650 each having a thickness of 15  $\mu\text{m}$ . Then,

electroplating is performed on the following conditions, thereby forming electroplated films 652 each having a thickness of 15  $\mu\text{m}$  (Fig. 41(A)). It is noted that additive contained in an

15 electroplating solution is Kaparacid HL manufactured by Atotech Japan.

#### [Electroplating Solution]

Sulfuric acid                            2.24 mol/l

Copper sulfate                        0.26 mol/l

Additive (Kaparacid HL                19.5 mol/l

manufactured by Atotech Japan)

#### [Electroplating Conditions]

Current density                        1 A/dm<sup>2</sup>

Duration                                65 minutes

Temperature                             $22 \pm 2^\circ\text{C}$

(15) After separating and removing the resists 650 with 5% NaOH, the Ni-Cu metal layers 648 under the plating resists are dissolved and removed by etching using a solution mixture of a nitric acid, a sulfuric acid and hydrogen peroxide, thereby forming conductor

circuits 758 each consisting of the Ni-Cu metal layer 648 and the electroplated film 652 and a plurality of relatively small via holes 760 connected onto the via hole 660 (Fig. 41(B)). In this embodiment, the via hole 660 is formed to have a filled 5 via hole structure, thereby making it possible to directly connect a plurality of via holes 760 to the via hole 660.

Later steps are the same as those of (16) to (19) in the first embodiment stated above, which description will not be, therefore, given herein.

10 Next, description will be given to the mounting of the IC chip on the printed circuit board 610 completed through the above-stated steps (Fig. 42) and to the attachment of the printed circuit board to the daughter board, with reference to Fig. 43. The IC chip 690 is mounted on the printed circuit board 610 thus 15 completed so that the solder pads 692 of the IC chip 690 correspond to the solder bumps 676U of the printed circuit board 610 and a reflow process is performed, thereby mounting the IC chip 690 on the printed circuit board 610. Likewise, a reflow process is performed so that the pads 694 of the daughter board 695 20 correspond to the solder bumps 676D of the printed circuit board 610, thereby attaching the printed circuit board 610 to the daughter board 695.

The above-stated resin contains a refractory resin, soluble particles, a hardening agent and other components, each 25 of which is the same as that described in the first embodiment and will not be described herein.

#### [First Modification of Fourth Embodiment]

Next, a printed circuit board 612 according to the first 30 modification of the fourth embodiment of the present invention will be described with reference to Fig. 52. In the fourth embodiment stated above, description has been given to a case

of arranging the BGA. The first modification of the fourth embodiment is almost the same as the fourth embodiment. However, as shown in Fig. 52, the printed circuit board in this modification is constituted into a PGA system establishing connection through 5 conductive connection pins 696.

Next, a method of manufacturing the printed circuit board stated above with reference to Fig. 32 will be described with reference to Figs. 45 to 52.

(1) First, a through hole 733a for containing chip capacitors 10 are formed in a multilayer plate 730 $\alpha$  constituted by providing four bonding resin layers 638 impregnated with an epoxy resin. Also, a multilayer plate 730 $\beta$  constituted by providing two bonding resin layers 638 is prepared (Fig. 45(A)). Here, as 15 the bonding resin layers 638, those containing a BT resin, a phenol resin or a reinforcing material such as glass cloth in addition to the epoxy resin can be employed.

(2) Next, the multilayer plates 730 $\alpha$  and 730 $\beta$  are press-contacted with each other, heated and hardened, thereby forming a core substrate 630 provided with a concave portion 20 735 capable of containing a plurality of chip capacitors 620 (Fig. 45(B)).

(3) Then, using potting (dispenser), a bonding material 636 is applied to the positions of the concave portion 735 at which the capacitors are to be arranged (Fig. 45(C)). Alternatively, 25 the bonding material can be applied to the concave portion by a printing method, a die-bonding method, a method of applying bonding sheets or the like. Thereafter, a plurality of chip capacitors 620 made of ceramic are contained in the concave portion 735 through the bonding material 636 (Fig. 45(D)).

(4) Then, a thermosetting resin is filled between the chip capacitors 620 within the concave portion 735, heated and hardened, thereby forming a resin layer 633 (Fig. 46(A)). At

this time, as the thermosetting resin, an epoxy resin, a phenol resin, a polyimide resin or a triazine resin is preferable. As a result, the chip capacitors 620 within the concave portion 735 can be fixed.

5 (5) Further, using a printer, the epoxy or polyolefin resin described above is applied onto the resultant substrate to thereby form a resin insulating layer 640 (Fig. 46(B)).

Alternatively, a resin film may be bonded instead of applying a resin.

10 (6) Next, openings 639 for relatively large via holes are formed in the resin insulating layer 640 by exposure and development processes or by applying laser (Fig. 46(C)). The diameters of the relatively large via holes are preferable in a range of 100 to 600  $\mu\text{m}$ . Especially, the relatively large are

15 preferable in a range of 125 to 350  $\mu\text{m}$ . In this case, the via holes are each formed to have a diameter of 165  $\mu\text{m}$ . Holes 644 for through holes each having a diameter of 250  $\mu\text{m}$  are formed in the resin layer 633 by drilling or by applying laser, heated and hardened (Fig. 46(D)).

20 (7) A palladium catalyst is applied to the substrate 630. Then, the core substrate is immersed in an electroless plating solution to uniformly deposit electroless plated films 745 (Fig. 47(A)). Then, resin filler is filled in the openings 639 on which the electroless plated films 745 are respectively formed, and dried.

25 By doing so, a resin layer 747 is formed in each opening 639 (Fig. 47(B)).

(8) Thereafter, photosensitive dry films are bonded to the surfaces of the electroless plated films 745, masks are mounted thereon, exposure and development processes are performed, 30 thereby forming resists 649 each having a predetermined pattern. The core substrate 630 is then immersed in an electroless plating solution, thereby forming plated covers 751 each consisting of

an electroless plated film (Fig. 47(C)).

(9) After the above step, the resists 649 are separated with 5% NaOH. Thereafter, the electroless plated films 745 under the resists 649 are etched away with a solution mixture of a 5 sulfuric acid and hydrogen peroxide, thereby forming relatively large via holes 661 of a filled via hole structure and through holes 656 (Fig. 47(D)). By constituting the via holes 661 to have the filled via hole structure, it is possible to directly connect a plurality of via holes 760 to one via hole 661 in a 10 step to be described later.

(10) After the substrate 630 is washed and degreased with an acid, the substrate 630 is subjected to soft-etching. Then, an etching solution is sprayed on the both sides of the substrate 630 to etch the surfaces of the via holes 661 and the land surfaces and inner walls of the through holes 656, thereby forming rough surfaces 663 on the entire surfaces of the via holes 661 and the through holes 656 (Fig. 48(A)). As the etching solution, an etching solution containing 10 parts by weight of an imidazole copper (II) complex, 7 parts by weight of a glycolic acid and 15 5 parts by weight of potassium chloride (MEC etch BOND 20 manufactured by Mec Company Ltd.) is employed.

(11) Next, 100 parts by weight of bisphenol F epoxy monomer (YL983U having a molecular weight of 310 and manufactured by Yuka Shell), 170 parts by weight of SiO<sub>2</sub> spherical particles 25 having a surface coated with a silane coupling agent, having a mean particle diameter of 1.6 µm and having a maximum particle diameter of 15 µm or less (CRS 11-1-CE manufactured by ADTEC) and 1.5 parts by weight of a leveling agent (PERENOL S4 manufactured by SANNOPCO) are stirred and mixed to thereby 30 prepare resin filler 664 having a viscosity of 45 to 49 Pa·s at 23±1°C. As a hardening agent, 6.5 parts by weight of an imidazole hardening agent (2E4MZ-CN manufactured by Shikoku

Chemicals) is employed.

Thereafter, the resin filler 664 is filled in the through holes 656 and dried (Fig. 48(B)).

(12) Next, 30 parts by weight of a bisphenol A epoxy resin (Epicoat 1001 having an epoxy equivalent of 469 and manufactured by Yuka Shell), 40 parts by weight of a cresol novolac epoxy resin (Epichron N-673 having an epoxy equivalent of 215 and manufactured by Dainippon Ink & Chemicals) and 30 parts by weight of a phenol novolac resin containing triazine structure (Phenolight KA-7052 having a phenol hydroxyl group equivalent of 120 and manufactured by Dainippon Ink & Chemicals) are heated and dissolved in 20 parts by weight of ethyl diglycol acetate and 20 parts by weight of solvent naphtha while being stirred. Then, 15 parts by weight of polybutadiene rubber having epoxy terminal (Denalex R-45EPT manufactured by Nagase Chemicals), 1.5 parts by weight of pulverized 2-phenyl-4, 5 bis(hydroxymethyl) imidazole, 2 parts by weight of particle-size reduced silica and 0.5 parts by weight of a silicon defoaming agent are added thereto, thus preparing an epoxy resin composition.

The obtained epoxy resin composition is applied onto a PET film having a thickness of 38  $\mu\text{m}$  by using a roll coater so that the thickness of the film is 50  $\mu\text{m}$  after the film is dried, and dried at 80 to 120°C for 10 minutes, thereby manufacturing resin films for interlayer resin insulating layers.

(13) The resin films for forming interlayer resin insulating layers slightly larger than the substrate 630 manufactured in (12) are mounted on the both sides of the substrate, respectively, temporarily pressed on conditions of a pressure of 4 kgf/cm<sup>2</sup>, a temperature of 80°C and a press duration of 10 seconds, and cut. Then, the resin films are bonded using a vacuum laminator device by the following method, thereby forming interlayer resin

insulating layers 740 (Fig. 48(C)). Namely, the interlayer resin insulating films are actually pressed on the substrate 630 on conditions of the degree of vacuum of 0.5 Torr, a pressure of 4 kgf/cm<sup>2</sup>, a temperature of 80°C and a press duration of 60

5 seconds and then thermally hardened at 170°C for 30 minutes.

(14) Next, openings 642 for relatively small via holes of 65 µm are formed in the interlayer resin insulating layers 740 by applying CO<sub>2</sub> gas laser through masks 757 in which penetrating holes 757a each having a thickness of 1.2 mm (Fig. 48(D)) are

10 formed. The diameters of the relatively small via holes are preferably in a range of 25 to 100 µm.

(15) The substrate 630 having the via hole openings 642 formed therein is immersed in a solution containing 60 g/l of a permanganate acid at a temperature of 80°C for 10 minutes and epoxy resin particles existing on the surfaces of the interlayer resin insulating layers 740 are dissolved and removed, thereby forming rough surfaces 646 on the surfaces of the interlayer resin insulating layers 740 including the inner walls of the via hole openings 642 (Fig. 49(A)). The roughing process may

20 be performed using an acid or an oxidizer. The rough surfaces are preferably 0.5 to 5 µm.

(16) Next, the substrate 630, for which the above stated processes have been completed, is immersed in a neutral solution (manufactured by Sipley) and washed. A palladium catalyst is applied to the surfaces of the substrate 630 which surfaces have been roughed (with a rough depth of 3 µm), thereby attaching catalyst cores on the surfaces of the interlayer resin insulating layers 740 and the inner wall surfaces of the via hole openings 642.

25 30 (17) Then, the substrate 630 is immersed in an electroless copper plating solution having the following composition to form electroless copper plated films 763 each having a thickness of

0.6 to 3.0 $\mu$ m on the entire rough surfaces 646 (Fig. 49(B)).

[Electroless Plating Solution]

NiSO <sub>4</sub>	0.003 mol/l
Tartaric acid	0.200 mol/l
Copper sulfate	0.030 mol/l
HCHO	0.050 mol/l
NaOH	0.100 mol/l
$\alpha, \alpha'$ -bipyridyl	40 mg/l
Polyethylene glycol (PEG)	0.10 g/l

5 [Electroless Plating Conditions]

40 minutes at a solution temperature of 35°C.

(18) Commercially available photosensitive dry films are bonded onto the electroless copper plated films 763, masks are mounted thereon, respectively and the films are exposed with 100 mJ/cm<sup>2</sup> and developed with a 0.8% sodium carbonate solution, thereby providing plating resists 650 each having a thickness of 30  $\mu$ m. Then, the resultant substrate 630 is washed with water of a temperature of 50°C and degreased, washed with water of a temperature of 25°C and with a sulfuric acid, and subjected to electroplating on the following conditions, thereby forming electroplated copper films 652 each having a thickness of 20  $\mu$ m (Fig. 49(C)).

20 [Electroplating Solution]

Sulfuric acid	2.24 mol/l
Copper sulfate	0.26 mol/l
Additive	19.5 mol/l
(Kaparacid HL manufactured by Atotech Japan)	

[Electroplating Conditions]

Current density	1 A/dm <sup>2</sup>
Duration	65 minutes
temperature	22±2 °C

(19) After separating and removing the plating resists 650 with 5% NaOH, the electroless plated films 763 under the plating resists 650 are etched with a solution mixture of a sulfuric acid and hydrogen peroxide, removed and dissolved, thereby forming conductor circuits 758 and relatively small via holes 760 each consisting of the electroless copper plated film 763 and the electroplated copper film 652 and having a thickness 10 of 18 µm (Fig. 49(D)). The same process as that in (10) is performed, i.e., rough surfaces 622 are formed by employing an etching solution containing a cupric complex and an organic acid (Fig. 50(A)).

(20) The steps of (13) to (19) are repeated, thereby forming 15 interlayer resin insulating layers 741, conductor circuits 759 and via holes 764 further above (Fig. 50(B)).

(21) Next, a solder resist composition (an organic resin insulating material) is obtained in the same manner as that in the first embodiment.

(22) Then, the solder resist composition prepared in (21) is applied to each side of the multilayer printed board to have a thickness of 20 µm. After a drying process is performed on conditions of 70°C for 20 minutes and 70°C for 30 minutes, a photomask having a thickness of 5 mm on which the pattern of 25 solder resist openings are drawn, is closely attached to each solder resist composition, exposure is performed with ultraviolet rays of 1000 mJ/cm<sup>2</sup>, development is performed with a DMTG solution to thereby form openings 671U and 671D.

Thereafter, a heating process is performed to harden the

solder resist composition on conditions of 80°C for 1 hour, 100°C for 1 hour, 120°C for 1 hour and 150°C for 3 hours to thereby harden the solder resist composition and form solder resist layers 670 each having openings 671U and 671D and having a thickness of 20 µm (Fig. 51(A)). The solder resist composition may be a commercially available solder resist composition.

(23) Then, the substrate 630 having the solder resist layers 670 formed thereon is immersed in the same electroless nickel plating solution as that employed in the first embodiment, thereby forming a nickel plated layer 672 in each of the openings 671U and 671D. Further, the substrate is immersed in the same electroless gold plating solution as that employed in the first embodiment, thereby forming a gold plated layer 674 having a thickness of 0.03 µm on the nickel plated layer 672 (Fig. 51(B)).

(24) Thereafter, a solder paste containing tin-lead is printed on each opening 671U of the solder resist layers 670 on the side of the substrate on which the IC chip is mounted. Further, a solder paste as a conductive bonding agent 697 is printed in each opening 671 on the other side of the substrate. Next, conductive connection pins 696 are attached to and supported by an appropriate pin holding device and the fixed portions 698 of the respective conductive connection pins 696 are brought into contact with the conductive bonding agent 697 within the openings 671D. After a reflow process is performed, the conductive connection pins 696 are attached to the conductive bonding agent 697. Also, to attach the conductive connection pins 696, the conductive bonding agent 697 may be formed into a ball shape or the like and put in the openings 671D, or the conductive bonding agent 697 may be joined to the fixed portions 698 to attach the conductive connection pins 696, followed by a reflow process.

Thereafter, the IC chip 690 is mounted on the printed

circuit board 612 so that the solder pads 692 of the IC chip 690 correspond to the opening 671U side-solder bumps 676U of the printed circuit board 612, and a reflow process is performed, thereby attaching the IC chip 690 (Fig. 53).

5

[Second Modification of Fourth Embodiment]

A printed circuit board according to the second modification of the fourth embodiment of the present invention will be described with reference to Fig. 53. A printed circuit board 614 in the second modification of the fourth embodiment is almost the same as that in the fourth embodiment stated above. However, in the printed circuit board 614 in the second modification of the fourth embodiment, one chip capacitor 620 is contained in the concave portion 736 formed in the core substrate 630. Since the chip capacitor 620 is arranged within the core substrate 630, the distance between the IC chip 690 and the chip capacitor 620 becomes short and loop inductance can be reduced.

20 [Third Modification of Fourth Embodiment]

Next, the constitution of a printed circuit board according to the third modification of the fourth embodiment will be described with reference to Fig. 14.

The printed circuit board in the third modification is almost the same in constitution as the printed circuit board in the first embodiment stated above. They, however, differ in chip capacitors 20 contained in the core substrate 30. Fig. 14 is a plan view of chip capacitors. Fig. 14(A) shows a chip capacitor before being cut for providing a plurality of chip capacitors. In Fig. 14(A), a dashed line denotes a cut line. As shown in Fig. 14(B), in the printed circuit board in the first embodiment stated above, the first electrodes 21 and the second

electrodes 22 are provided on the edges of the chip capacitor. Fig. 14(C) shows a chip capacitor before being cut for providing a plurality of chip capacitors in the third modification. In Fig. 14(C), a dashed line denotes a cut line. In the printed circuit board in the third modification, as shown in the plan view of Fig. 14(D), first electrodes 21 and second electrodes 22 are provided inside of the edges of the chip capacitor.

In the printed circuit board in the third modification, the chip capacitors 20 each having electrodes formed inside of the outer edges thereof are employed, so that mass storage chip capacitors can be employed.

Next, a printed circuit board according to the first other example of the third modification will be described with reference to Fig. 15.

Fig. 15 is a plan view of a chip capacitor 20 contained in the core substrate of the printed circuit board according to the first other example. In the first embodiment stated above, a plurality of small storage chip capacitors are contained in the core substrate. In the first other example, by contrast, a large, mass storage chip capacitor 20 is contained. The chip capacitor 20 consists of the first electrodes 21, the second electrodes 22, a dielectric 23, first conductive films 24 connected to the first electrodes 21, second conductive films 25 connected to the second electrodes 22, electrodes 27 which are not connected to the first and second conductive films 24 and 25, for the connection of the upper and lower surfaces of the chip capacitor. The IC chip and the daughter board are connected to each other through the electrodes 27.

Since the large chip capacitor is employed in the printed circuit board in the first modification, it is possible to employ a mass storage chip capacitor. Further, since the large chip capacitor 20 is employed, the printed circuit board does not

warp even if a heat cycle is performed repeatedly.

A printed circuit board according to the second other example of the second modification will be described with reference to Fig. 16. Fig. 16(A) shows a chip capacitor before being cut for providing a plurality of chip capacitors. In Fig. 16(A), a dashed line denotes an ordinary cut line. Fig. 16(B) is a plan view of the chip capacitors. As shown in Fig. 16(B), a plurality of (or in Fig. 16(B), three) chip capacitors for providing multiple capacitors are coupled to one another and employed as a large capacitor as a whole.

In the second other example, since the large chip capacitor 20 is employed, it is possible to employ a mass storage chip capacitor. Further, since the large chip capacitor is employed, the printed circuit board does not warp even if a heat cycle is performed repeatedly.

In the embodiment stated above, the chip capacitors are built in the printed circuit board. Alternatively, plate-like capacitors each constituted by providing a conductive film on a ceramic plate may be employed instead of the chip capacitors.

Further, in the fourth embodiment stated above, only the chip capacitors contained in the core substrate are provided. Alternatively, mass storage chip capacitors can be mounted on the front and reverse sides of the substrate as in the case of the first other example of the first embodiment.

As described above with reference to Fig. 12, voltage variation can be minimized by providing the chip capacitors 20 in the vicinity of the IC chip and the mass storage chip capacitors (having relatively high inductance) on the front and reverse sides.

Now, as for the printed circuit board in the fourth embodiment, the measurement values of the inductance of the chip capacitor 620 embedded in the core substrate and that of the

chip capacitor mounted on the reverse side (daughter board side-surface) of the printed circuit board are shown below.

In a case where a single capacitor is used:

5	Embedded type	137 pH
	Reverse side mounted type	287 pH

In a case where eight capacitors are connected in parallel:

10	Embedded type	60 pH
	Reverse side mounted type	72 pH

As can be understood from the above, it is possible to reduce inductance by including the chip capacitor(s) regardless of whether a single capacitor is used or capacitors are connected in parallel so as to increase storage capacity.

Next, the result of a reliability test will be described. Here, the rate of change of the capacitance of one chip capacitor on the printed circuit board in the fourth embodiment was measured.

		Rate of Change of Capacitance	
		(measurement	(measurement
		frequency 100Hz)	frequency 1kHz)
Steam	168 hours	0.3%	0.4%
HAST	100 hours	-0.9%	-0.9%
TS	1000 cycles	1.1%	1.3%

In the Steam test, a humidity of 100% was maintained by applying steam. In the HAST test, the chip capacitor was left at a relative humidity of 100%, an applied voltage of 1.3 V and a temperature of 121°C for 100 hours. In the TS test, tests for leaving the capacitor at -125°C for 30 minutes and 55°C for

30 minutes were repeated 1000 times.

As a result of the above-stated reliability test, it was discovered that the printed circuit board including the chip capacitor(s) therein can attain equivalent reliability to that of the existing capacitor surface mount type. Further, as a result of the TS test, it was discovered that even if an internal stress occurs due to the difference in the coefficient of thermal expansion among the capacitors made of ceramic, the core substrate made of a resin and the interlayer resin insulating layers, disconnection does not occur between the electrodes of the chip capacitors and the via holes, separation does not occur between the chip capacitors and the interlayer resin insulating layers and cracks do not occur to the interlayer resin insulating layer, whereby high reliability can be attained for a long time.

With the constitution of the fourth embodiment, the via holes in the fourth embodiment are formed between the conductor circuits and the capacitors. Due to this, it is possible to maintain desired performance without delaying operation due to lack of power supply and no problems arose even if a reliability test was conducted.

Moreover, because of the via holes, even if the via holes are formed in the interlayer resin insulating layers and positional errors occur to the via holes, the allowance is wide. Thus, electrical connection characteristics can be ensured.

WHAT IS CLAIMED IS:

1. A printed circuit board constituted by alternately laminating interlayer resin insulating layers and conductive circuits on a core substrate containing a capacitor,

5 characterized in that

the core substrate containing said capacitor is constituted by providing a first resin substrate, a second resin substrate having an opening for containing the capacitor and a third resin substrate in a multilayer manner while interposing bonding plates.

10 2. A printed circuit board according to claim 1, wherein each of said bonding plates has a core impregnated with a thermosetting resin.

15 3. A printed circuit board according to claim 1 or 2, wherein each of said first, second and third resin substrates has a core impregnated with a resin.

20 4. A printed circuit board according to any one of claims 1 to 3, wherein

a plurality of said capacitors are provided.

25 5. A printed circuit board according to any one of claims 1 to 4, wherein

the conductor circuits are formed on said second resin substrate.

30 6. A printed circuit board according to any one of claims 1 to 5, wherein

the capacitor is mounted on a surface of said printed circuit board.

- G E D E E D E G E C P A C T I O N
7. A printed circuit board according to claim 6, wherein  
a capacitance of the chip capacitor on said surface is  
equal to or higher than a capacitance of a chip capacitor on  
5 an inner layer.
8. A printed circuit board according to claim 6, wherein  
an inductance of the chip capacitor on said surface is  
equal to or higher than an inductance of the chip capacitor on  
10 an inner layer.
9. A printed circuit board according to any one of claims  
1 to 8, wherein  
15 a metal film is formed on an electrode of said capacitor.
10. A printed circuit board according to claim 9, wherein  
the metal film formed on the electrode of said capacitor  
is a plated film mainly consisting of copper.
- 20 11. A printed circuit board according to claims 1 to 8, wherein  
at least a part of a coating layer of the electrode of  
said capacitor is exposed and electrically connected to the  
electrode exposed from said coating layer.
- 25 12. A printed circuit board according to any one of claims  
1 to 11, wherein  
a chip capacitor having electrodes formed inside of an  
outer edge is employed as said capacitor.
- 30 13. A printed circuit board according to any one of claims  
1 to 12, wherein  
a chip capacitor having electrodes formed in a matrix is

employed as said capacitor.

14. A printed circuit board according to any one of claims  
1 to 13, wherein

5 a plurality of chip capacitors for providing many  
capacitors are coupled to be employed as said capacitor.

15. A printed circuit board according to claim 1, wherein  
said first resin substrate and said capacitor are coupled  
10 to each other by an insulating bonding agent and the insulating  
bonding agent is lower in a coefficient of thermal expansion  
than said first resin substrate.

16. A printed circuit board manufacturing method  
15 characterized by comprising at least the following steps (a)  
to (d):

(a) forming a conductor pad section on a first resin substrate;  
(b) connecting a capacitor to said conductor pad section of  
said first resin substrate through a conductive bonding agent;  
20 (c) providing a third resin substrate, a second resin substrate  
having an opening for containing said capacitor and said first  
resin substrate in a multilayer manner while interposing bonding  
plates so that said capacitor of said first resin substrate is  
contained in said opening of said second resin substrate and  
25 that said opening of said second resin substrate is closed by  
the third resin substrate; and  
(d) heating and pressurizing said first resin substrate, said  
second resin substrate and said third resin substrate, to thereby  
provide a core substrate.

30 17. A printed circuit board constituted by providing resin  
insulating layers and conductor circuits on a core substrate

in a multilayer manner, characterized in that  
said core substrate is constituted by bonding together  
a plurality of resin substrates, the conductor circuits formed  
on said plurality of resin substrates; and  
5 a capacitor is contained in said core substrate.

18. A printed circuit board constituted by providing resin  
insulating layers and conductor circuit on a core substrate in  
a multilayer manner, characterized in that

10 said core substrate is constituted by bonding together  
a plurality of resin substrates, the conductor circuits formed  
on said plurality of resin substrates; and  
a capacitor is contained in a concave portion formed in  
said core substrate.

15 19. A printed circuit board according to claim 17 or 18, wherein  
said plurality of resin substrates are bonded together by  
interposing bonding plates.

20 20. A printed circuit board according to claim 19, wherein  
each of said bonding plate has a core impregnated with  
a thermosetting resin.

25 21. A printed circuit board according to any one of claims  
17 to 20, wherein  
each of said resin substrates has a core impregnated with  
a resin.

22. A printed circuit board according to any one of claims  
30 17 to 21, wherein  
a plurality of said capacitors are provided.

23. A printed circuit board according to any one of claims 17 to 21, wherein

the capacitor is mounted on a surface of said printed circuit board.

5

24. A printed circuit board according to claim 23, wherein a capacitance of a chip capacitor on said surface is equal to or higher than a capacitance of a chip capacitor on an inner layer.

10

25. A printed circuit board according to claim 23, wherein an inductance of a chip capacitor on said surface is equal to or higher than an inductance of the chip capacitor on an inner layer.

15

26. A printed circuit board according to any one of claims 17 to 25, wherein a metal film is formed on an electrode of said capacitor and is electrically connected to the electrode on which said metal film is formed, by plating.

20

27. A printed circuit board according to claim 26, wherein the metal film formed on the electrode of said capacitor is a plated film mainly consisting of copper.

25

28. A printed circuit board according to claims 17 to 27, wherein

at least a part of a coating layer of the electrode of said capacitor is exposed and electrically connected to the electrode exposed from said coating layer.

30

29. A printed circuit board according to any one of claims 17 to 28, wherein

DE2020200000000000

a chip capacitor having electrodes formed inside of an outer edge is employed as said capacitor.

30. A printed circuit board according to any one of claims  
5 17 to 29, wherein

a chip capacitor having electrodes formed in a matrix is employed as said capacitor.

31. A printed circuit board according to any one of claims  
10 17 to 30, wherein

a plurality of chip capacitors for providing many capacitors are coupled to be employed as said capacitor.

32. A printed circuit board according to claim 17 or 18, wherein  
15 the capacitor is coupled to said core substrate by an insulating bonding agent and the insulating bonding agent is lower in a coefficient of thermal expansion than said core substrate.

20 33. A printed circuit board manufacturing method characterized by comprising at least the following steps (a) to (e):

(a) forming conductor circuits on a plurality of resin substrates;

25 (b) providing a plurality of said resin substrates in a multilayer manner through bonding plates;

(c) bonding together said resin substrates through said bonding plates, to thereby provide a core substrate;

(d) forming a concave portion in said core substrate; and

30 (e) containing a capacitor in said concave portion.

34. A printed circuit board manufacturing method comprising

at least the following steps (a) to (e):

- (a) forming a resin substrate with a through hole and having a conductor circuit provided on a surface;
- 5 (b) forming a resin substrate without a through hole and having a conductor circuit provided on a surface;
- (c) providing said resin substrate with the through hole and said resin substrate without the through hole through a bonding plate in a multilayer manner;
- 10 (d) bonding together said resin substrates through said bonding plate, to thereby provide a core substrate; and
- (e) containing a capacitor in said concave portion.

35. A printed circuit board constituted by alternately providing interlayer resin insulating layers and conductor circuits in a multilayer manner on a core substrate containing 15 a capacitor, characterized in that

the core substrate containing said capacitor is constituted by providing a first resin substrate, a second resin substrate having an opening for containing the capacitor and 20 a third resin substrate in a multilayer manner while interposing bonding plates; and

via holes connected to a terminal of said capacitor are provided on both sides of said core substrate.

25 36. A printed circuit board according to claim 35, wherein each of said bonding plates has a core impregnated with a thermosetting resin.

30 37. A printed circuit board according to claim 35 or 36, wherein each of said first, second and third resin substrates has a core impregnated with a resin.

38. A printed circuit board according to any one of claims  
35 to 37, wherein

a plurality of said capacitors are provided.

5 39. A printed circuit board according to any one of claims  
35 to 38, wherein

the conductor circuits are formed on said second resin  
substrate.

10 40. A printed circuit board according to any one of claims  
35 to 39, wherein

the capacitor is mounted on a surface of said printed  
circuit board.

15 41. A printed circuit board according to claim 40, wherein  
a capacitance of a chip capacitor on said surface is equal  
to or higher than a capacitance of a chip capacitor on an inner  
layer.

20 42. A printed circuit board according to claim 40, wherein  
an inductance of a chip capacitor on said surface is equal  
to or higher than an inductance of the chip capacitor on an inner  
layer.

25 43. A printed circuit board according to any one of claims  
35 to 42, wherein

wherein a metal film is formed on an electrode of said  
capacitor and is electrically connected to the electrode on which  
said metal film is formed, by plating.

30

44. A printed circuit board according to claim 43, wherein  
the metal film formed on the electrode of said capacitor

is a plated film mainly consisting of copper.

45. A printed circuit board according to claims 35 to 42,  
wherein

5 at least a part of a coating layer of the electrode of  
said capacitor is exposed and electrically connected to the  
electrode exposed from said coating layer.

46. A printed circuit board according to any one of claims  
10 35 to 45, wherein

a chip capacitor having electrodes formed inside of an  
outer edge is employed as said capacitor.

47. A printed circuit board according to any one of claims  
15 35 to 46, wherein

a chip capacitor having electrodes formed in a matrix is  
employed as said capacitor.

48. A printed circuit board according to any one of claims  
20 35 to 47, wherein

a plurality of chip capacitors for providing many  
capacitors are coupled to be employed as said capacitor.

49. A printed circuit board according to claim 35, wherein  
25 said first resin substrate and said capacitor are coupled  
to each other by an insulating bonding agent and the insulating  
bonding agent is lower in a coefficient of thermal expansion  
than said first resin substrate.

30 50. A printed circuit board manufacturing method  
characterized by comprising at least the following steps (a)  
to (d):

- (a) attaching a capacitor to a first resin substrate through  
a bonding material;
- (b) providing a third resin substrate, a second resin substrate  
having an opening for containing said capacitor and a first resin  
5 substrate in a multilayer manner so that said capacitor of said  
first resin substrate is contained in said opening of said second  
substrate and that said opening of said second resin substrate  
is closed by said third resin substrate, thereby providing a  
core substrate;
- 10 (c) applying laser and forming a via hole opening reaching  
said capacitor in said core substrate;
- (d) forming a via hole in said via hole opening.

51. A printed circuit board manufacturing method  
15 characterized by comprising at least the following steps (a)  
to (f):
- (a) forming a via hole formation opening in a metal film on  
one side of a first resin substrate;
- (b) attaching a capacitor to a metal film unformed surface  
20 of said first resin substrate through a bonding material;
- (c) providing a third resin substrate, a second resin substrate  
having an opening for containing said capacitor and said first  
resin substrate in a multilayer manner by interposing bonding  
plates so that said capacitor of said first resin substrate is  
25 contained in said opening of said second resin substrate and  
that said opening of said second resin substrate is closed by  
said third resin substrate;
- (d) heating and pressurizing said first resin substrate, said  
second resin substrate and said third resin substrate, to thereby  
30 provide a core substrate;
- (e) applying laser to said via hole formation opening formed  
in said metal film of said first resin substrate, and forming

a via hole opening reaching said capacitor; and  
(f) forming a via hole in said via hole opening.

52. A printed circuit board manufacturing method

5 characterized by comprising at least the following steps (a) to (f):

(a) forming via hole formation openings in metal films of a first resin substrate and a third resin substrate, the metal films bonded on one sides of said first resin substrate and said 10 third resin substrate, respectively;

(b) attaching a capacitor to a metal film unformed surface of said first resin substrate through a bonding material;

(c) providing said third resin substrate, a second resin substrate having an opening for containing said capacitor and 15 said first resin substrate in a multilayer manner by providing a bonding plate on said metal film unformed surface so that said capacitor of said first resin substrate is contained in said opening of said second resin substrate and that said opening of said second resin substrate is closed by said third resin 20 substrate;

(d) heating and pressurizing said first resin substrate, said second resin substrate and said third resin substrate, to thereby provide a core substrate;

(e) applying laser to said via hole formation openings formed 25 in said first resin substrate and said third resin substrate, and forming a via hole opening reaching said capacitor; and

(f) forming a via hole in said via hole opening.

53. A printed circuit board manufacturing method

30 characterized by comprising at least the following steps (a) to (g):

(a) forming a through hole formation openings in metal films

of a first resin substrate and a third resin substrate, the metal films bonded on one sides of said first resin substrate and said third resin substrate, respectively;

(b) attaching a capacitor to a metal film unformed surface  
5 of said first resin substrate through a bonding material;

(c) providing said third resin substrate, a second resin substrate having an opening for containing said capacitor and said first resin substrate in a multilayer manner by providing a bonding plate on said metal film unformed surface so that said  
10 capacitor of said first resin substrate is contained in said opening of said second resin substrate and that said opening of said second resin substrate is closed by said third resin substrate;

(d) heating and pressurizing said first resin substrate, said  
15 second resin substrate and said third resin substrate, to thereby provide a core substrate;

(e) applying laser to said through hole formation openings formed in said first resin substrate and said third resin substrate, and forming a via hole opening reaching said  
20 capacitor;

(f) removing or thinning said metal films; and

(g) forming a conductor circuit and a via hole on said core substrate.

25 54. A printed circuit board constituted by providing resin insulating layers and conductor circuits on a core substrate in a multilayer manner, characterized in that

a capacitor is included in said core substrate, and a relatively large lower-layer via hole connected to an electrode  
30 of said capacitor is formed; and

a plurality of relatively small upper-layer via holes connected to one said lower-layer via hole are provided in an

interlayer resin insulating layer on an upper surface of said core substrate.

55. A printed circuit board according to claim 54, wherein  
5 said lower-layer via hole is a filled via hole filled with  
an plated material and having a flat surface.

56. A printed circuit board according to claim 54, wherein  
10 said lower-layer via hole is a filled via hole having a  
resin filled inside and a metal film formed on a surface

57. A printed circuit board according to claim 54, wherein  
15 said capacitor is singularly contained in a concave portion  
formed in said core substrate.

58. A printed circuit board according to claim 54, wherein  
20 a plurality of said capacitors are contained in a concave  
portion formed in said core substrate.

59. A printed circuit board according to claim 54, wherein  
25 a metal film is formed on an electrode of said capacitor  
and electrically connected to the electrode on which said metal  
film is formed, by plating.

60. A printed circuit board according to claim 59, wherein  
30 the metal film formed on the electrode of said chip  
capacitor is a plated film mainly consisting of copper.

61. A printed circuit board according to claims 54 to 58,  
35 wherein  
at least a part of a coating layer of the electrode of  
said capacitor is exposed and electrically connected to the

electrode exposed from said coating layer.

62. A printed circuit board according to any one of claims  
54 to 61, wherein

5 a chip capacitor having electrodes formed inside of an  
outer edge is employed as said capacitor.

63. A printed circuit board according to any one of claims  
54 to 62, wherein

10 a chip capacitor having electrodes formed in a matrix is  
employed as said capacitor.

64. A printed circuit board according to any one of claims  
54 to 63, wherein

15 a plurality of chip capacitors for providing many  
capacitors are coupled to be employed as said capacitor.

65. A printed circuit board according to claim 54, wherein  
a resin lower, in a coefficient of thermal expansion, than  
20 the core substrate is filled between said core substrate and  
the capacitor.

66. A printed circuit board manufacturing method  
characterized by comprising at least the following steps (a)  
25 to (e):

- (a) embedding a capacitor in a core substrate;
- (b) forming a resin insulating layer on an upper surface of  
said capacitor;
- (c) forming a relatively large lower-layer via hole connected  
30 to an electrode of said capacitor, in said resin insulating layer;
- (d) forming an interlayer resin insulating layer on an upper  
surface of said core substrate; and

(e) providing a plurality of relatively small upper-layer via holes connected to one said lower-layer via hole, in said interlayer resin insulating layer.

5 67. A printed circuit board manufacturing method according to claim 66, comprising, before the step (a), a step of forming a concave portion in said core substrate and containing said capacitor in said concave portion.

10 68. A printed circuit board manufacturing method according to claim 66, comprising, before the step (a), a step of forming a concave portion in said core substrate and containing a plurality of said capacitors in said concave portion.

15 69. A printed circuit board manufacturing method according to claim 66, comprising, before the step (a), a step of forming a through hole in a resin plate, and bonding a resin plate to said resin plate on which said through hole is formed, to thereby form a core substrate having a concave portion.

20 70. A printed circuit board manufacturing method according to claim 66, wherein a filled via hole filled with a plated material and having a flat surface is formed when forming said lower-layer via hole.

25 71. A printed circuit board manufacturing method according to claim 66, wherein a filled via hole formed by filling a resin inside and then providing a metal film on a surface, is formed when forming said lower-layer via hole.

30 72. A printed circuit board manufacturing method according to claim 68, comprising, after the step (a), a step of applying

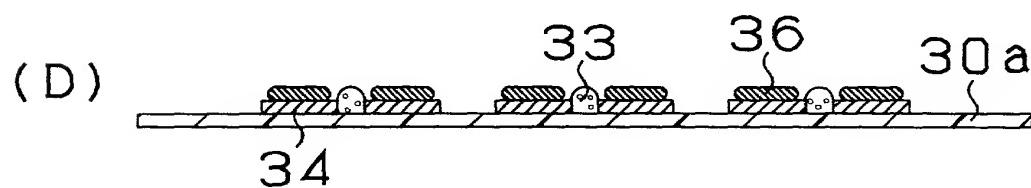
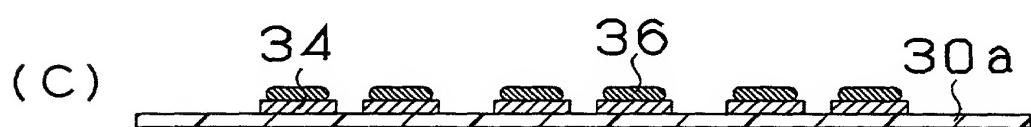
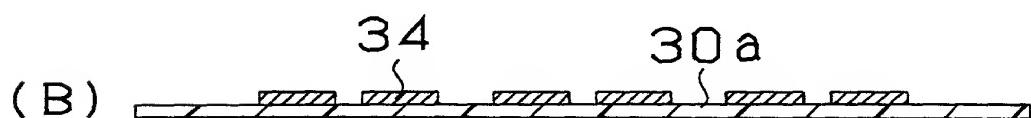
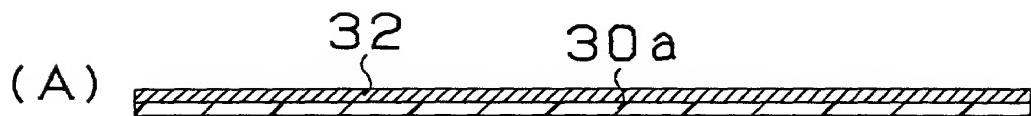
a pressure to upper surfaces of said plurality of capacitors within said concave portion from above, and making heights of the upper surfaces of said capacitors uniform.

## ABSTRACT

A chip capacitor 20 is provided in a core substrate 30 of a printed circuit board 10. This makes it possible to shorten a distance between an IC chip 90 and the chip capacitor 20 and 5 to reduce loop inductance. Since the core substrate 30 is constituted by providing a first resin substrate 30a, a second resin substrate 30b and a third resin substrate 30c in a multilayer manner, the core substrate 30 can obtain sufficient strength.

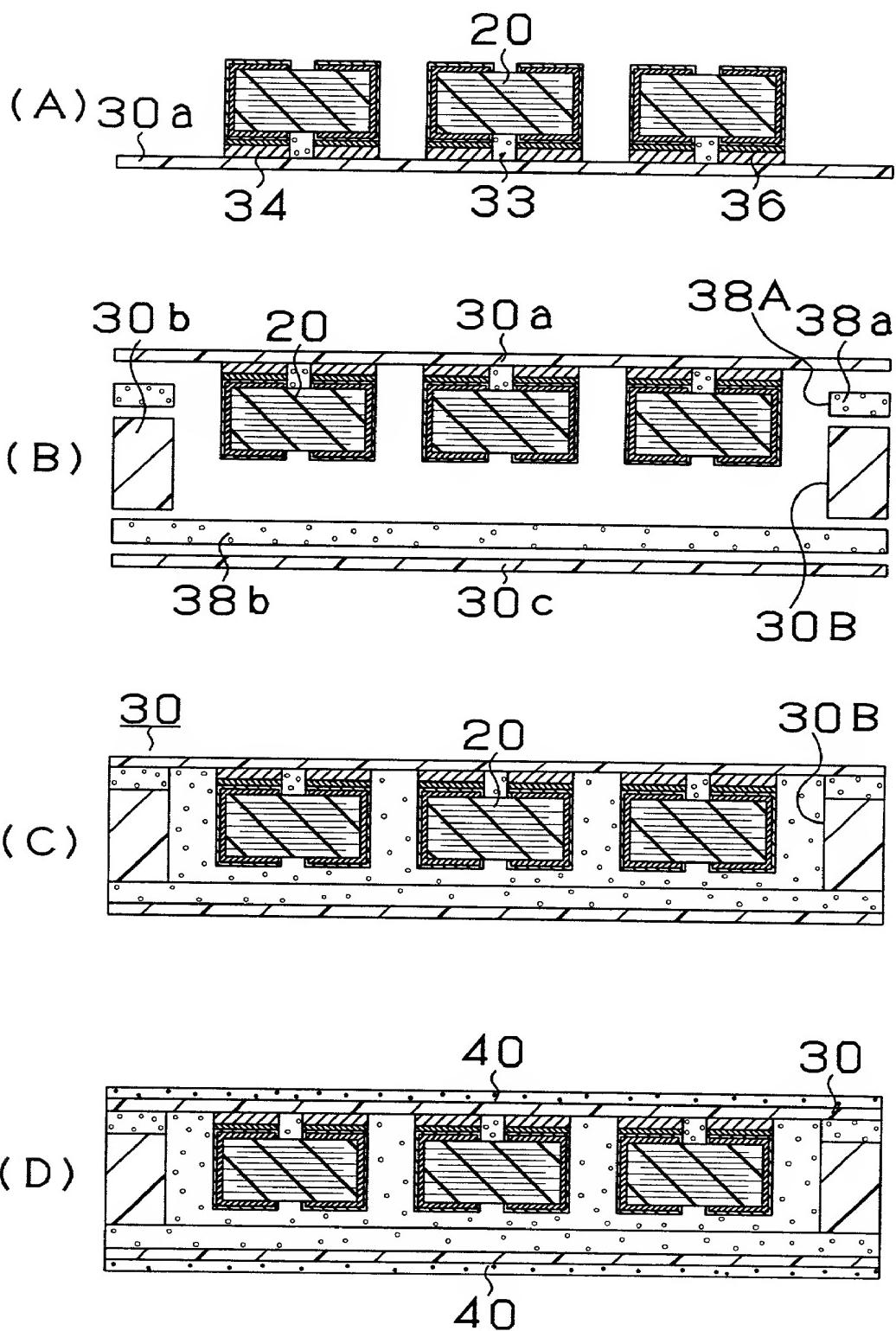
09/830360

1/53  
Fig. 1

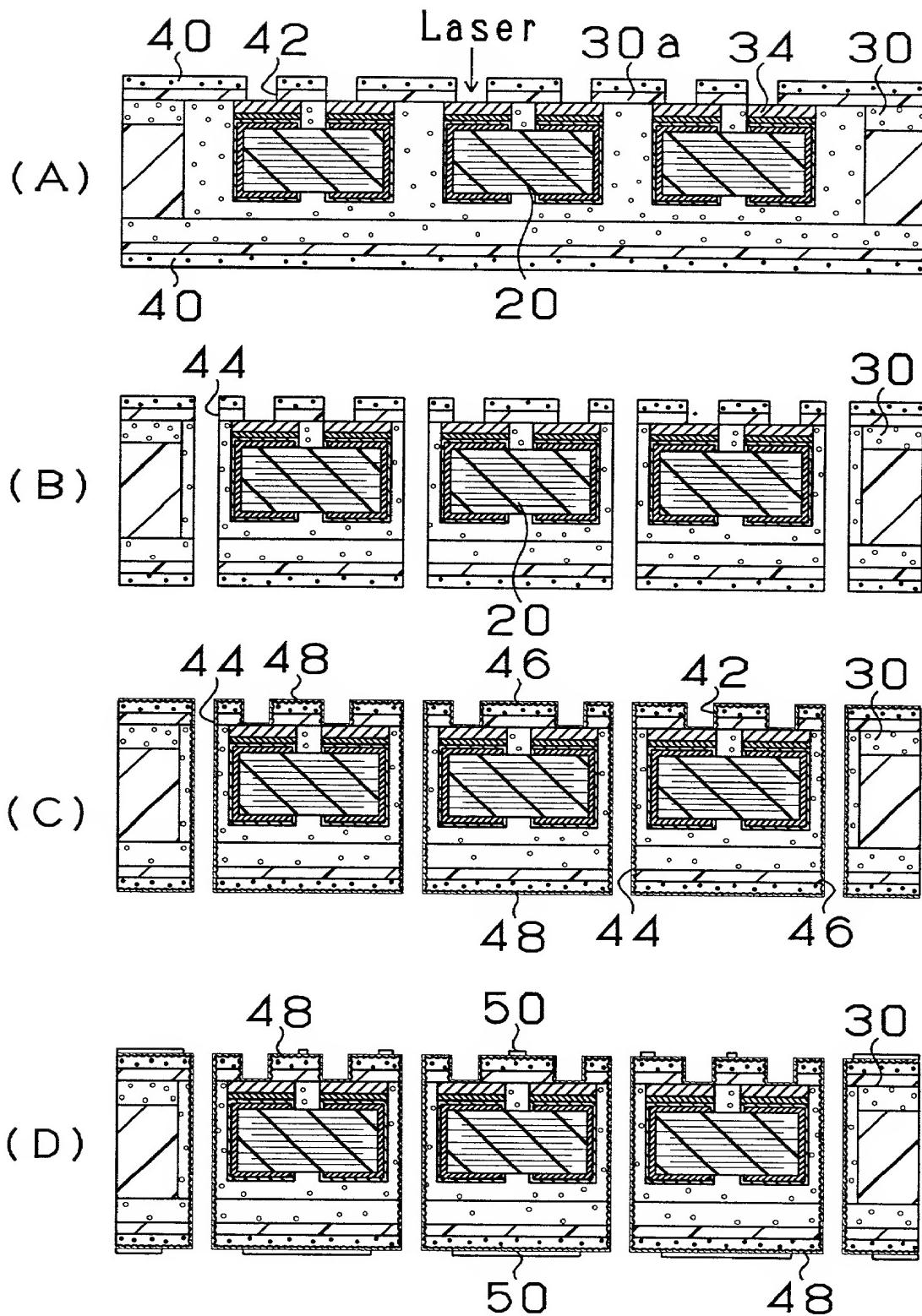


09/830360

2/53  
Fig. 2

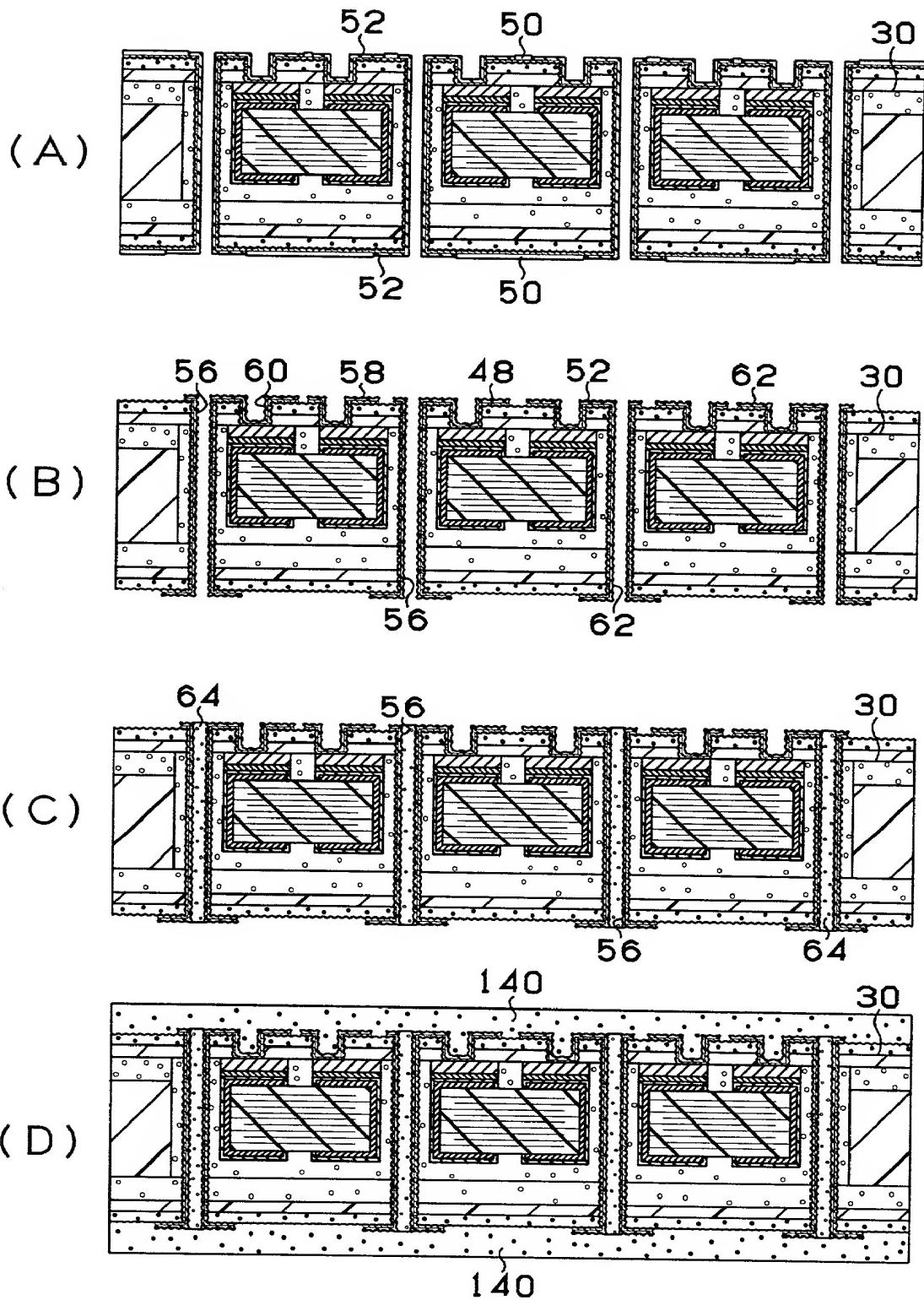


3/53  
Fig. 3



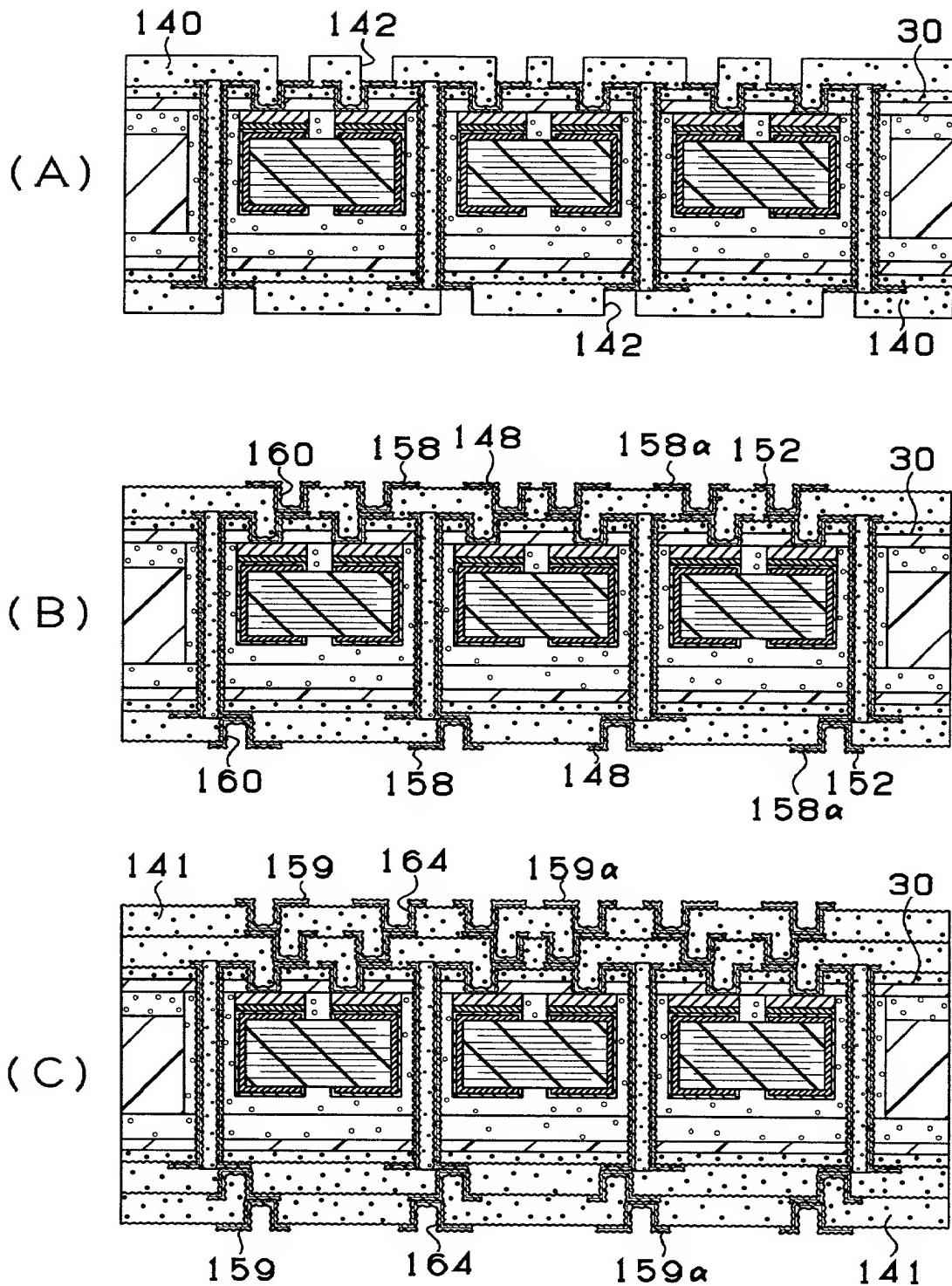
09/830360

4/53  
Fig. 4



09/830360

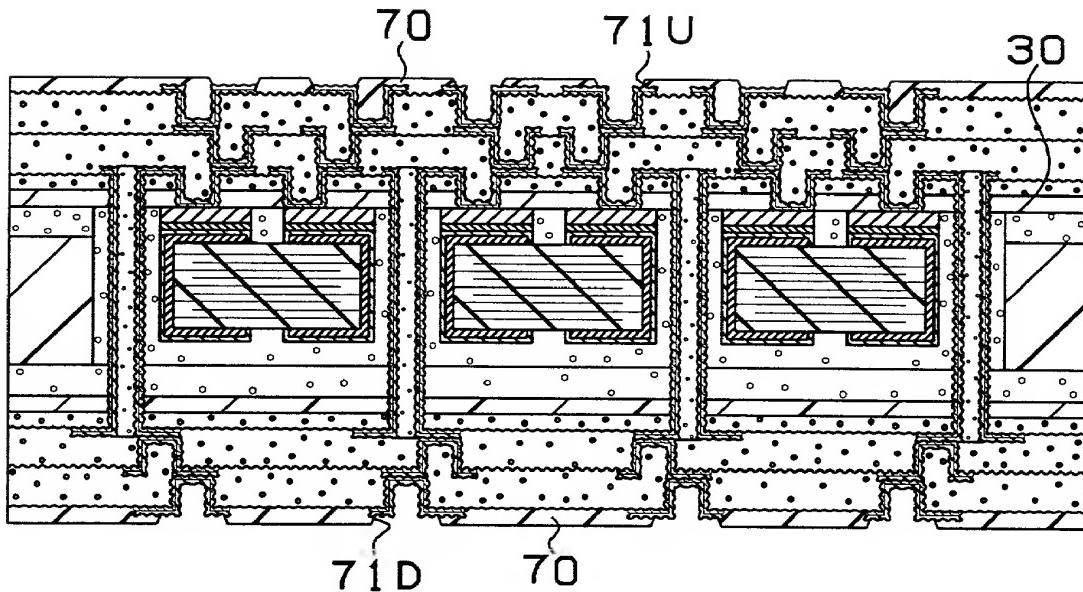
5/53  
Fig. 5



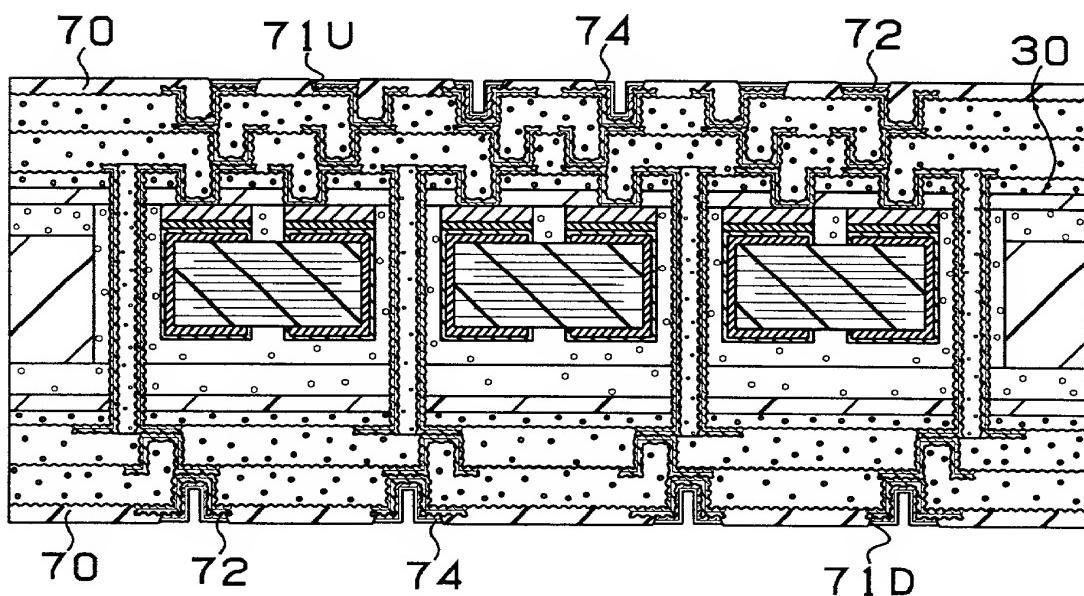
09/830360

6/53  
Fig. 6

(A)

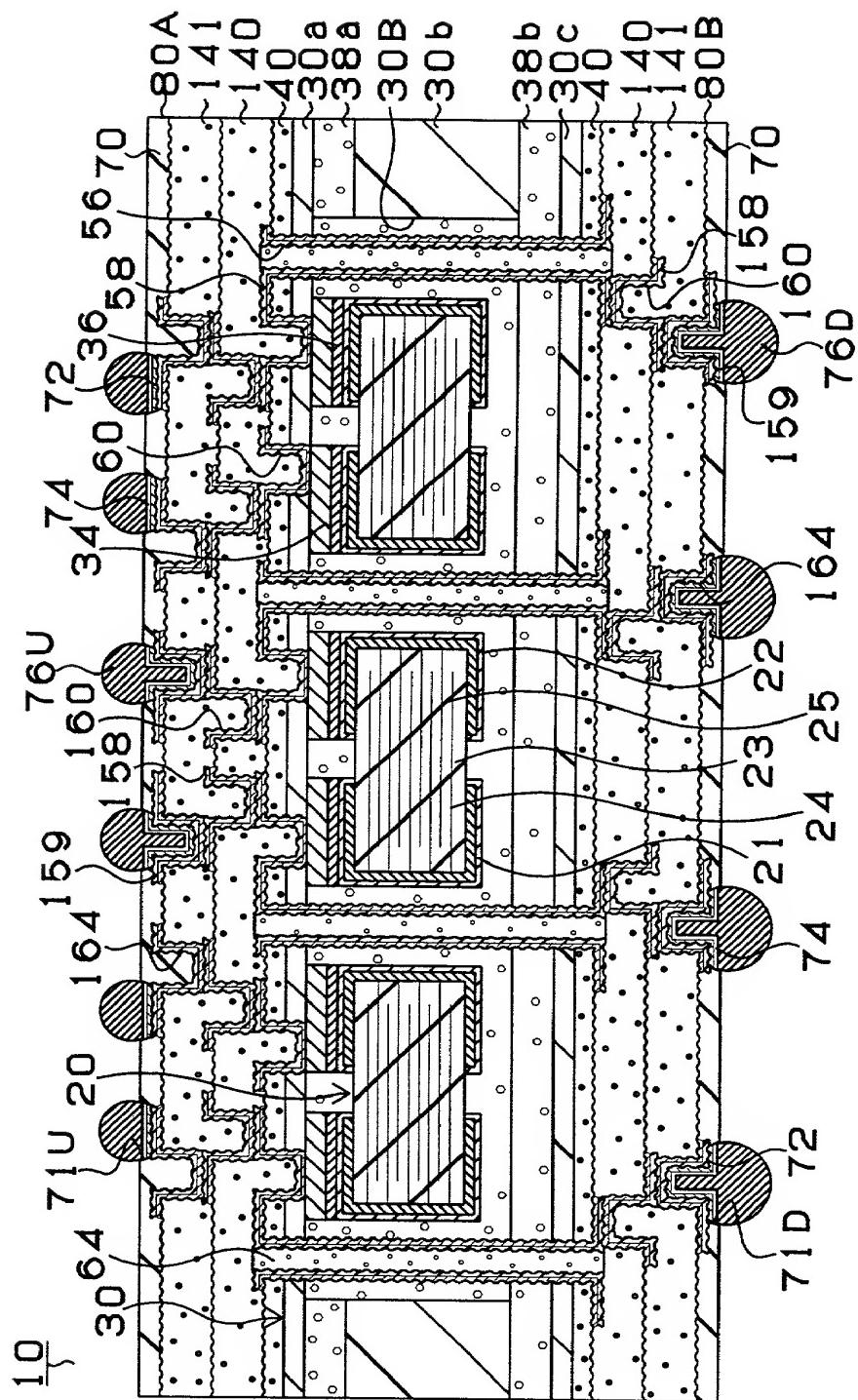


(B)



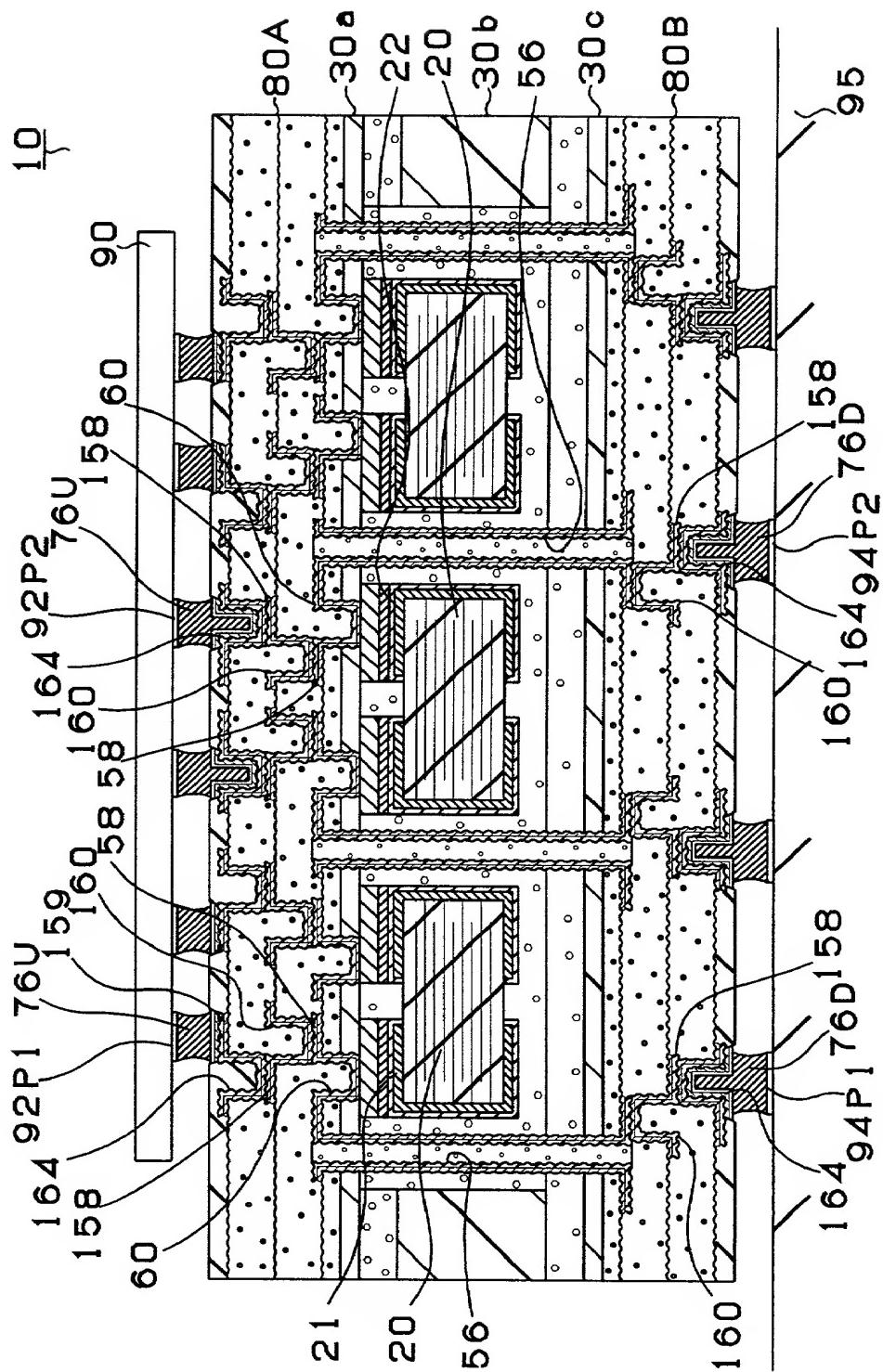
09/830360

7/53  
Fig. 7



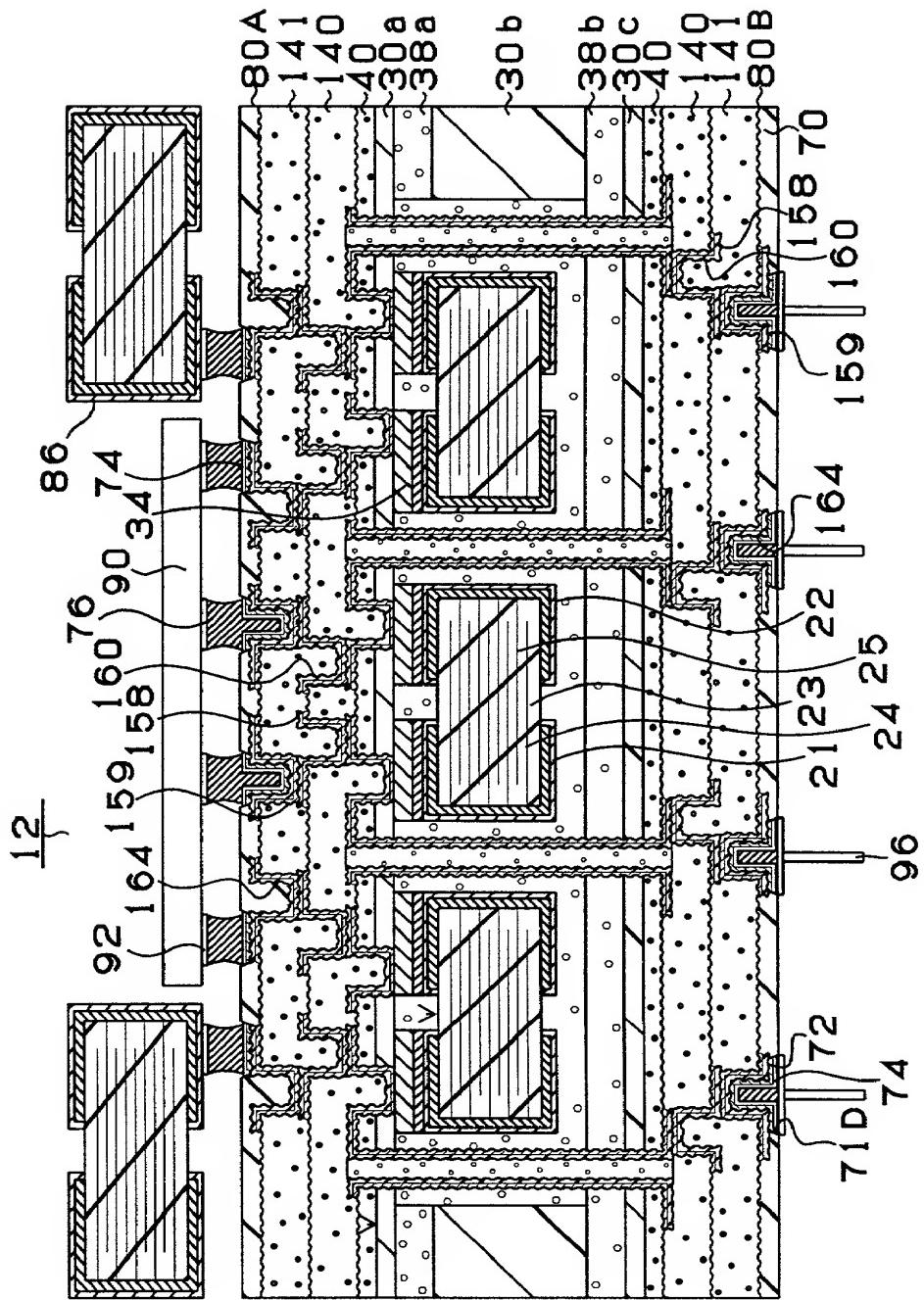
09/830360

Fig. 8  
8/53



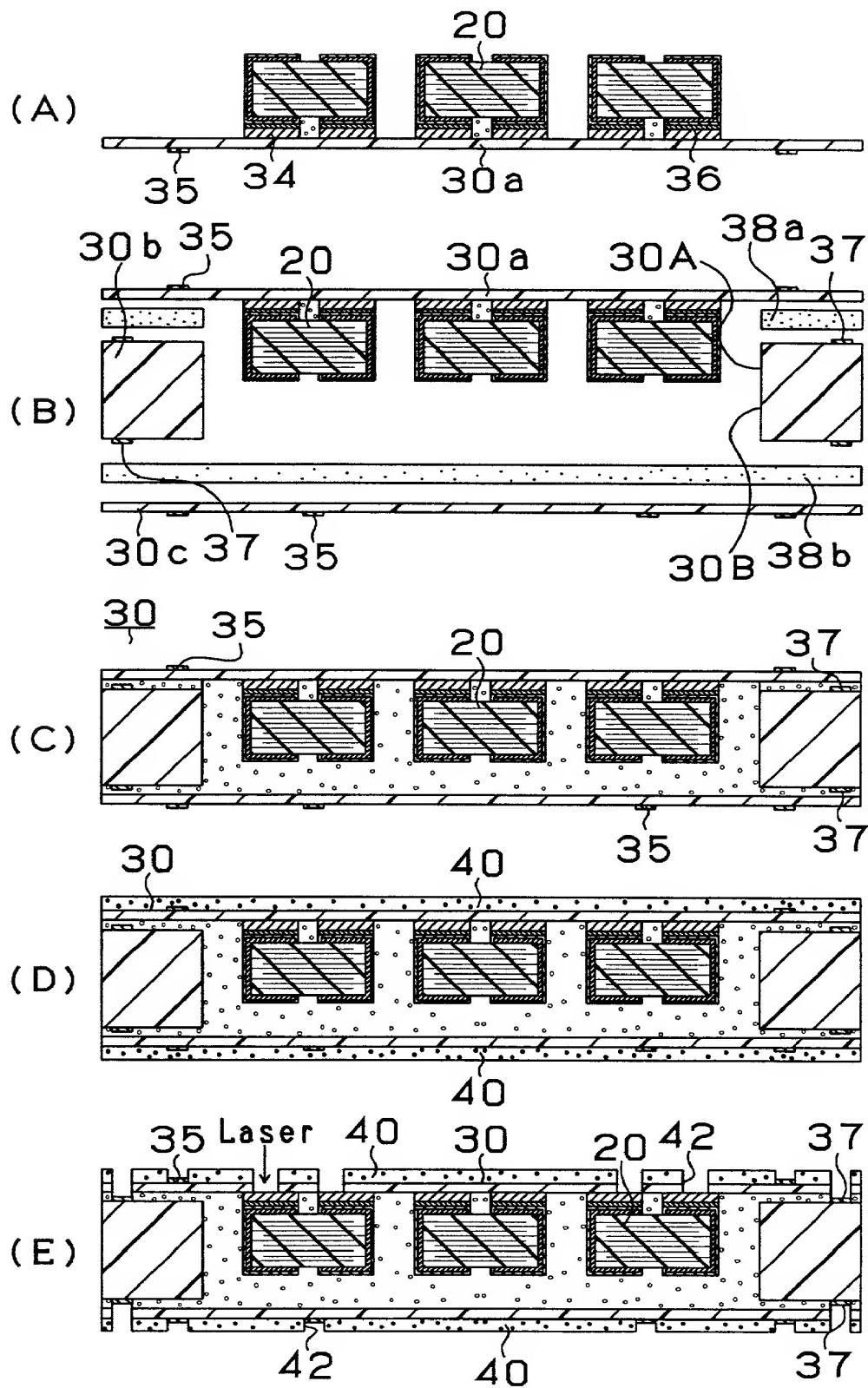
09/830360

Fig. 9  
9/53



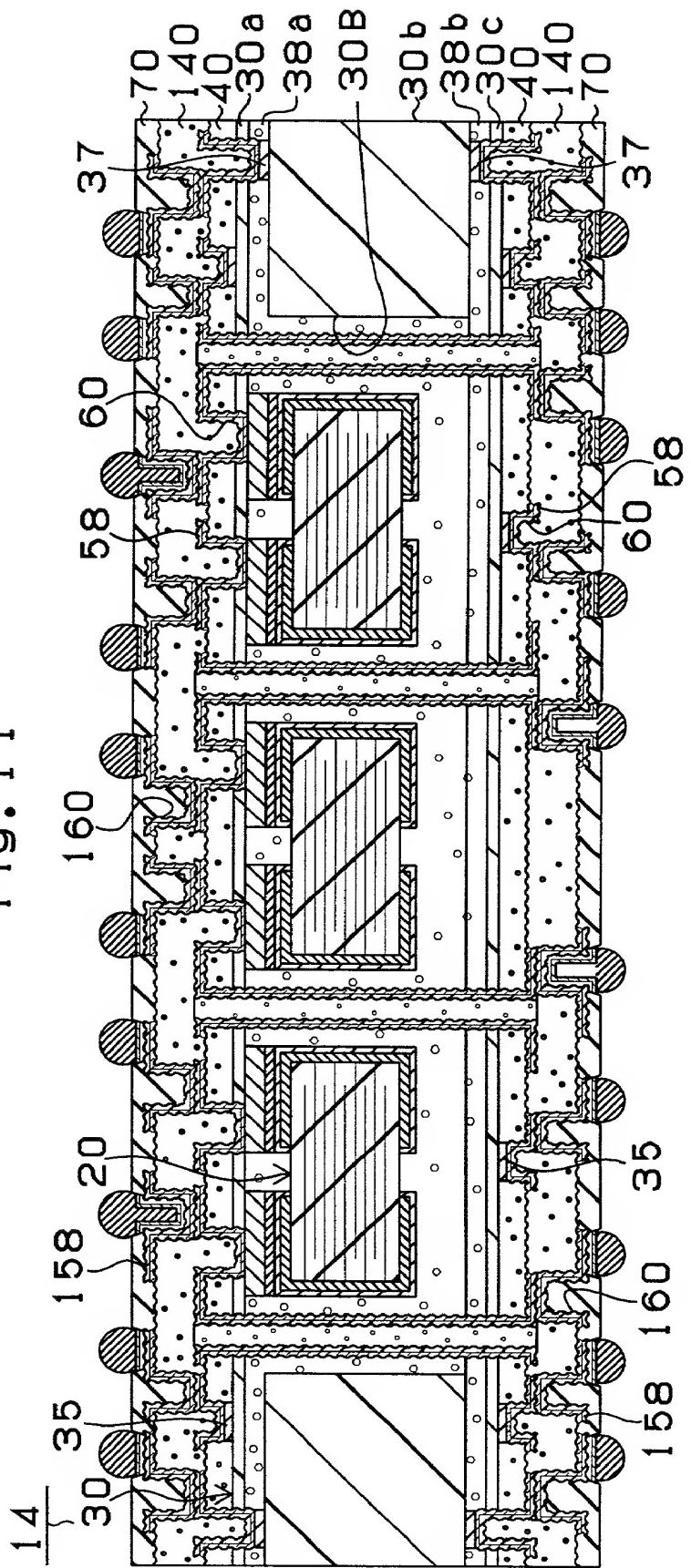
09/830360

10/53  
Fig. 10



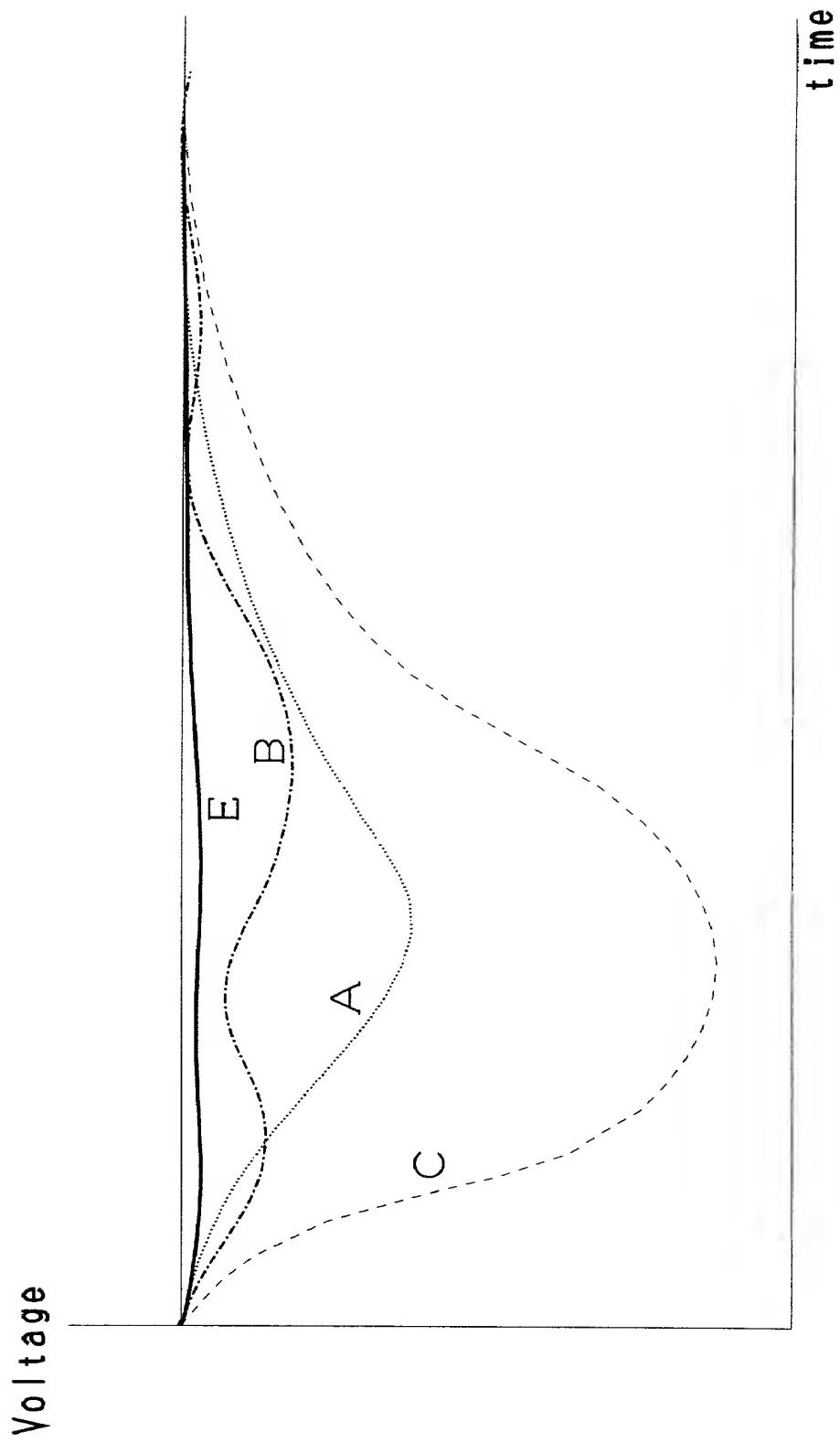
09/830360

11/53  
Fig. 11



09/830360

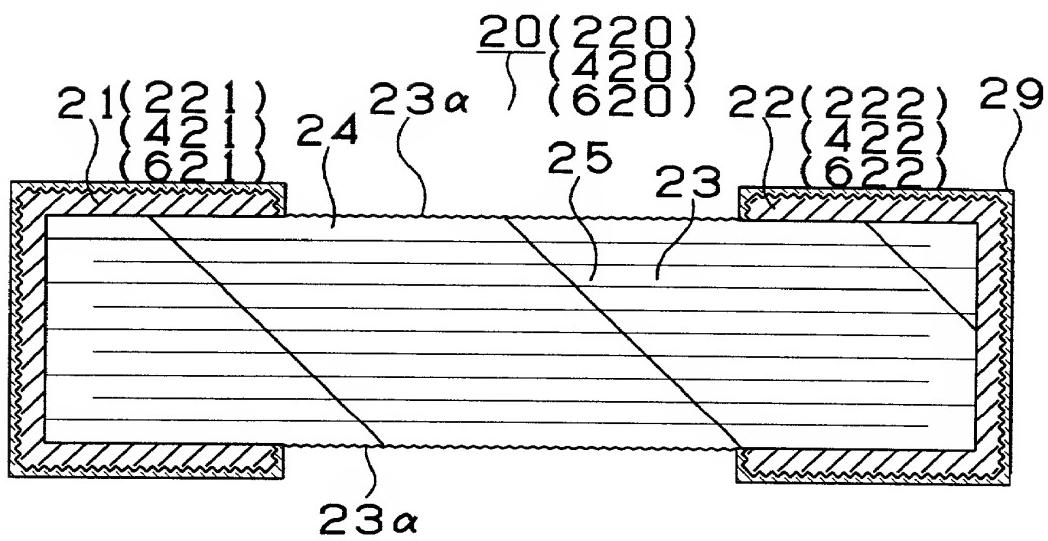
12/53  
Fig. 12



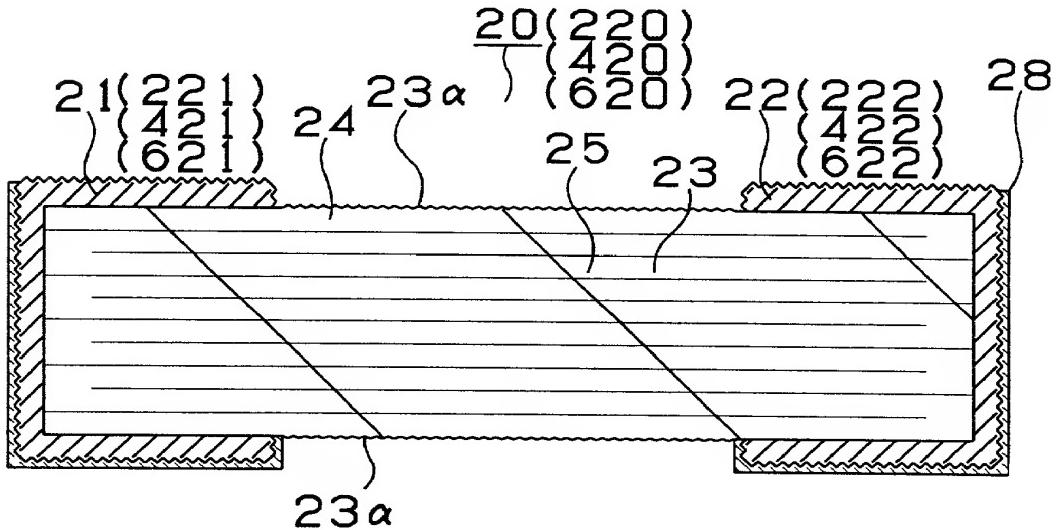
09/830360

13/53  
Fig. 13

(A)



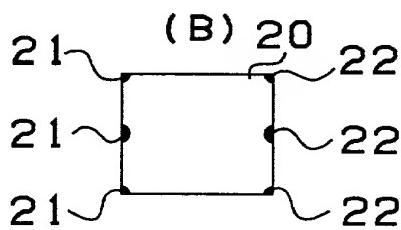
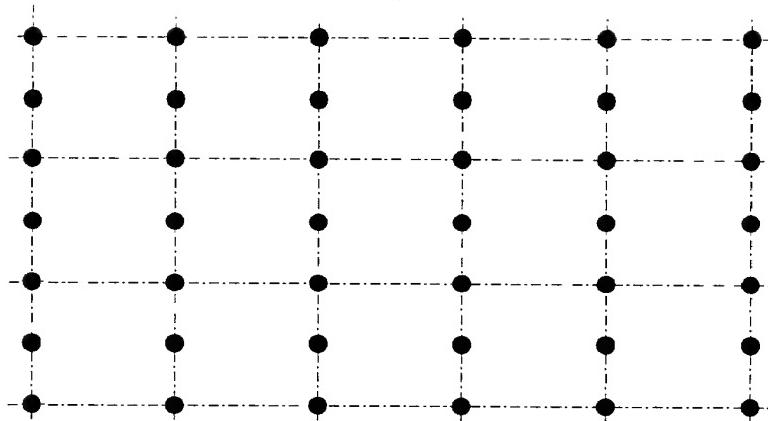
(B)



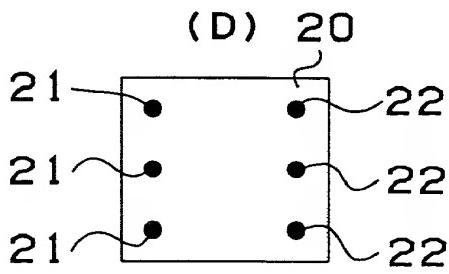
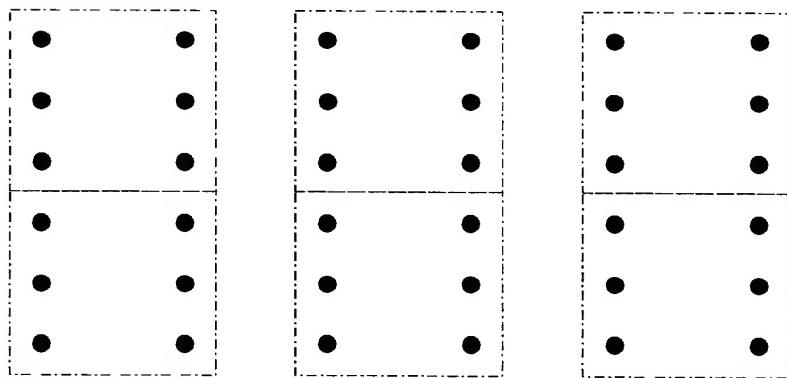
09/830360

14/53  
Fig. 14

(A)

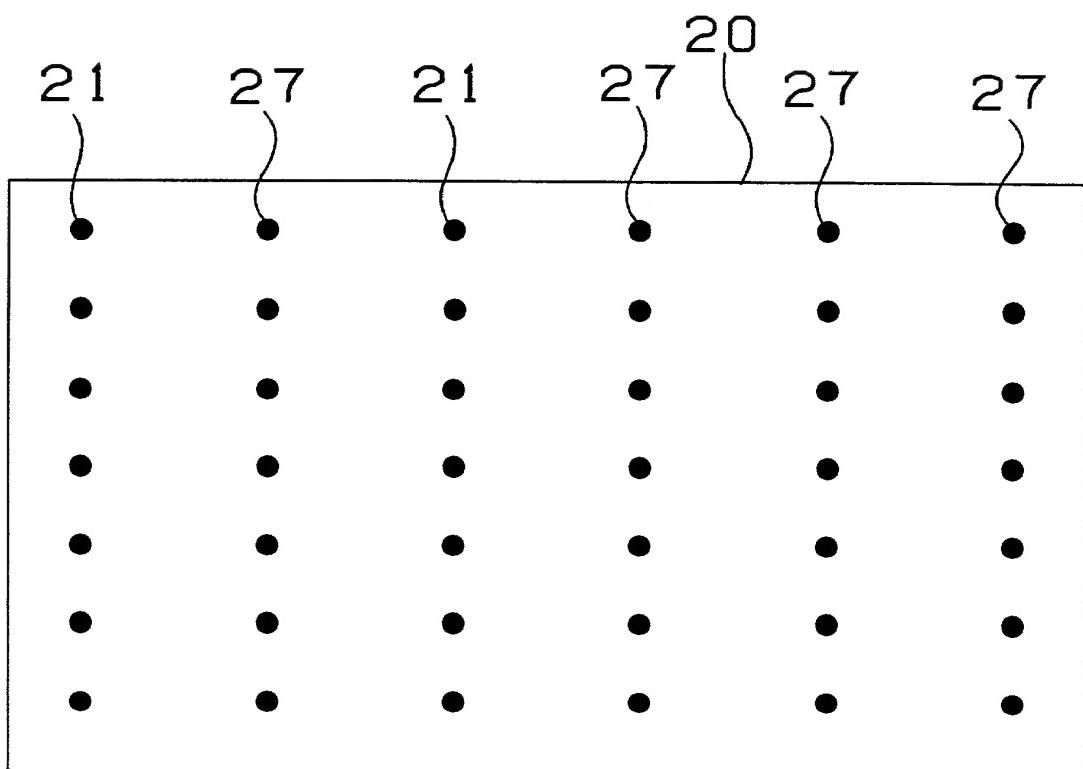


(C)



09/830360

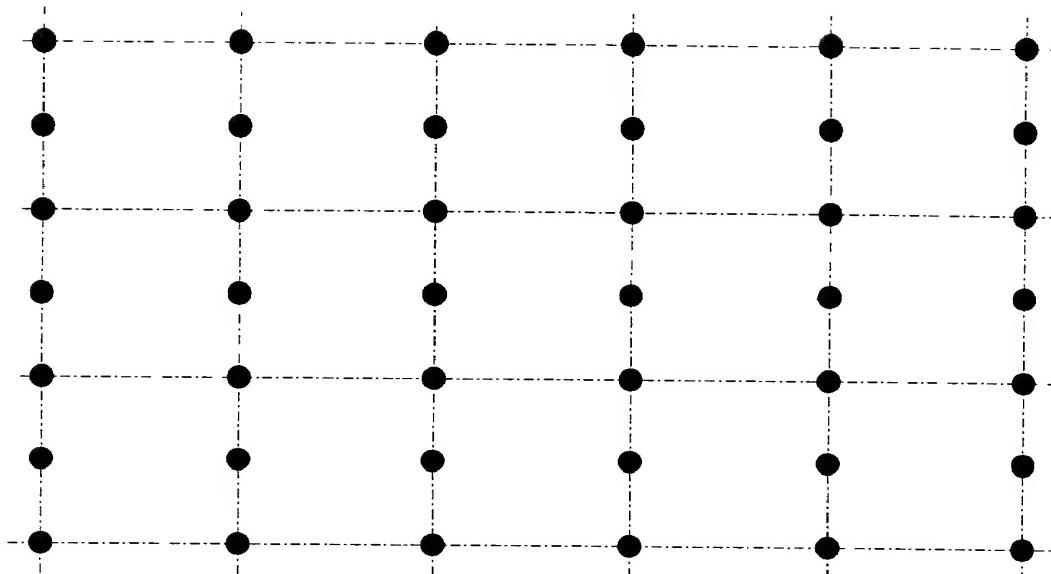
15/53  
Fig. 15



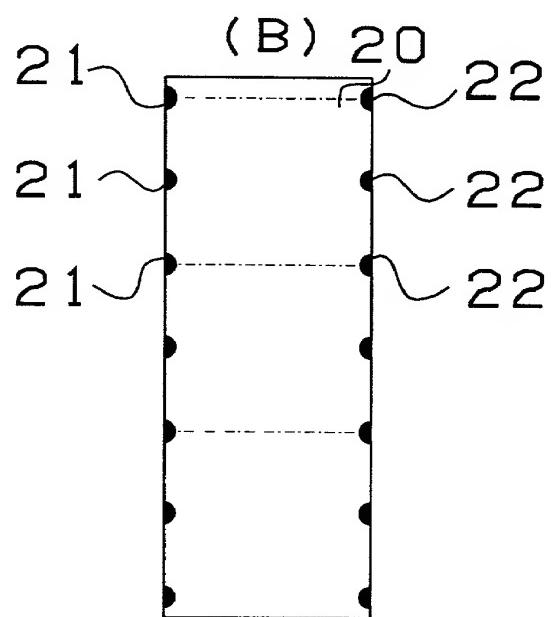
09/830360

16/53  
Fig. 16

(A)

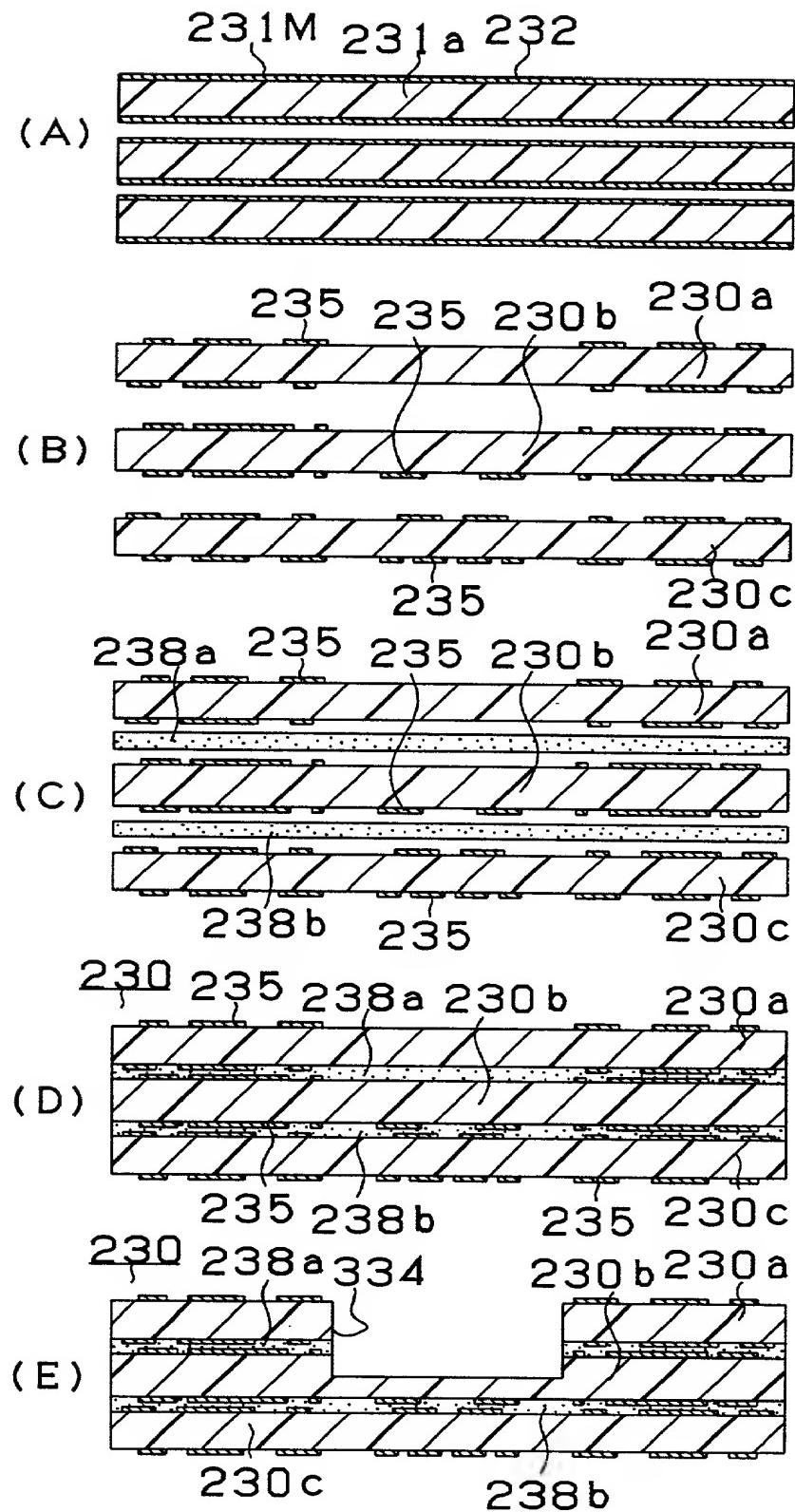


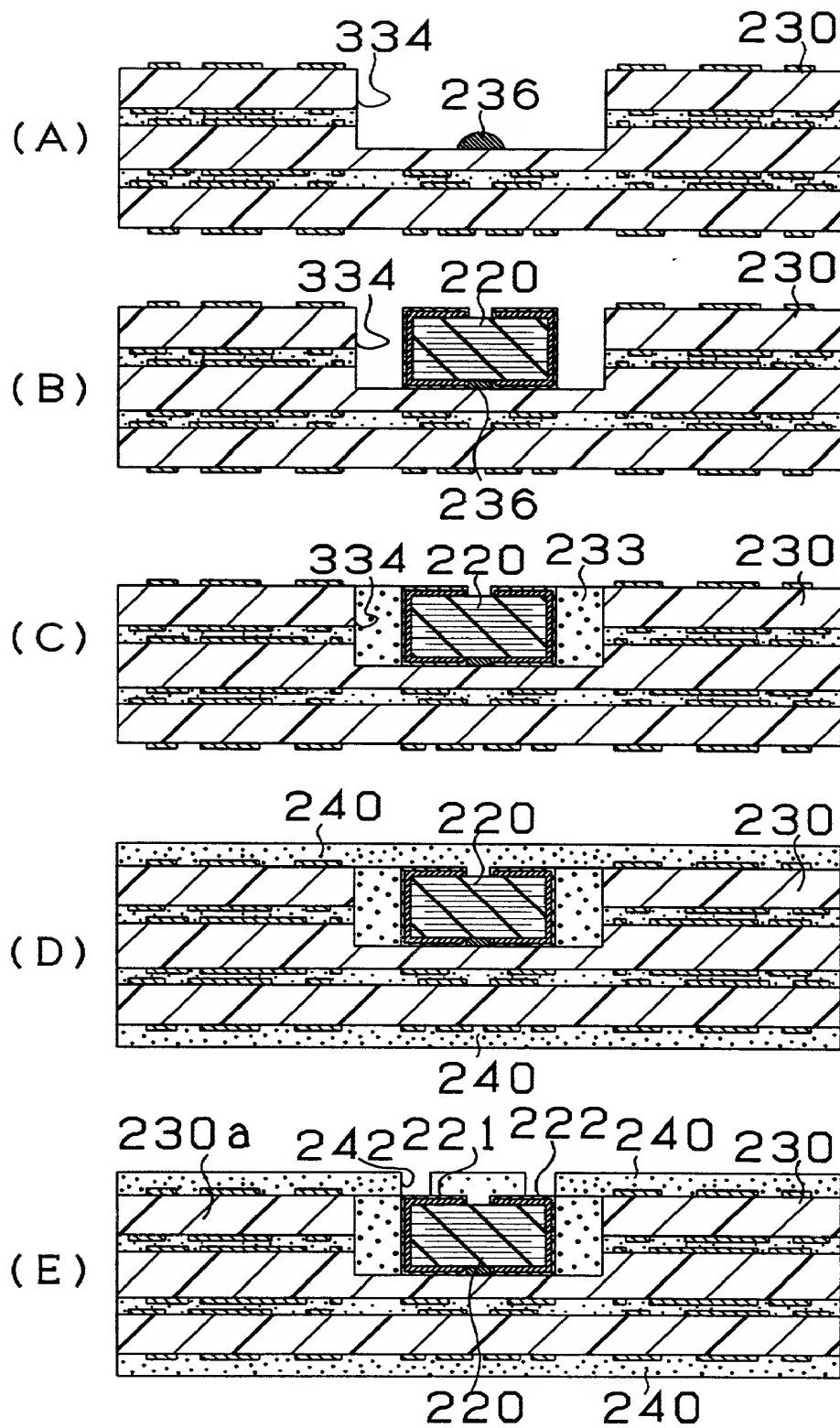
(B)



09/830360

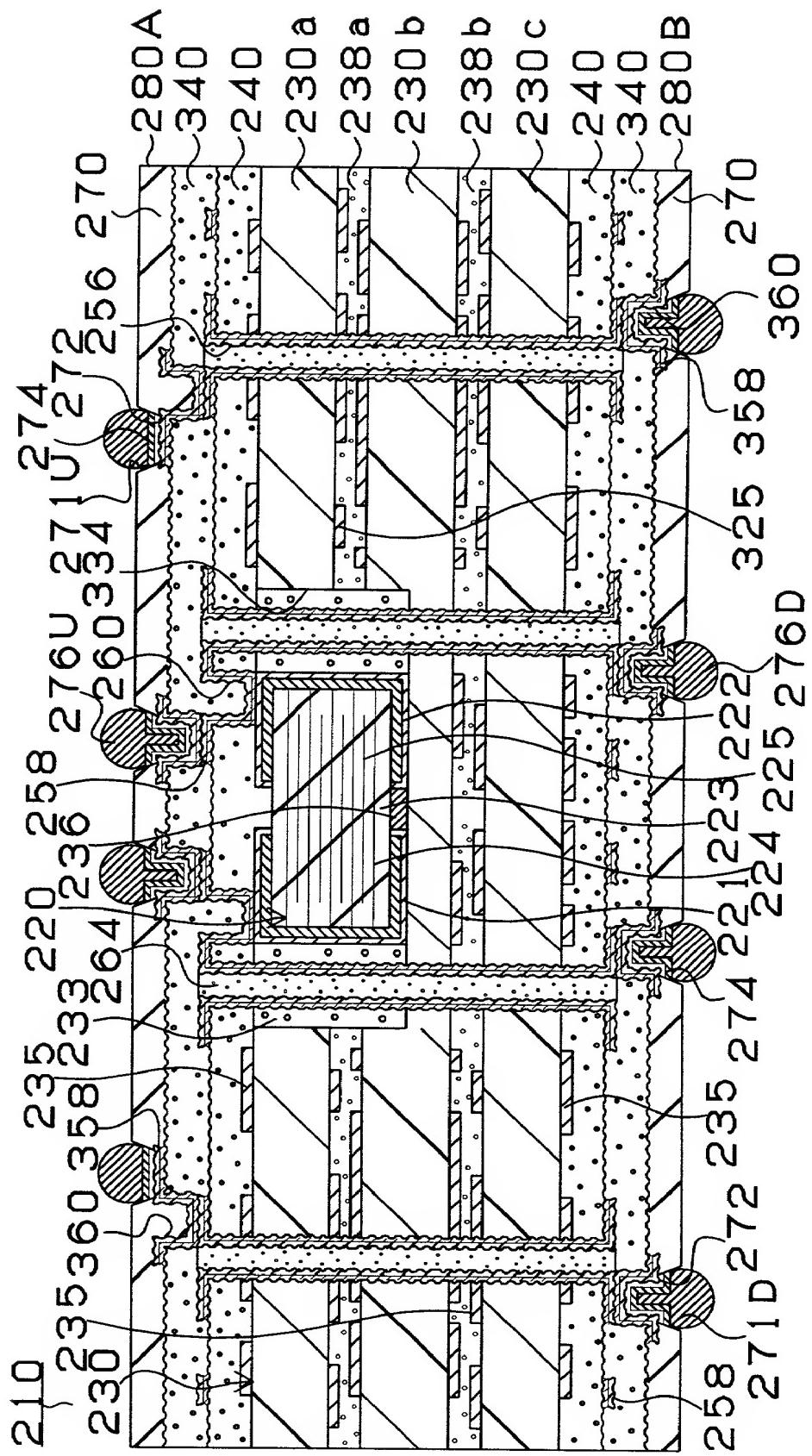
17/53  
Fig. 17



18/53  
Fig. 18

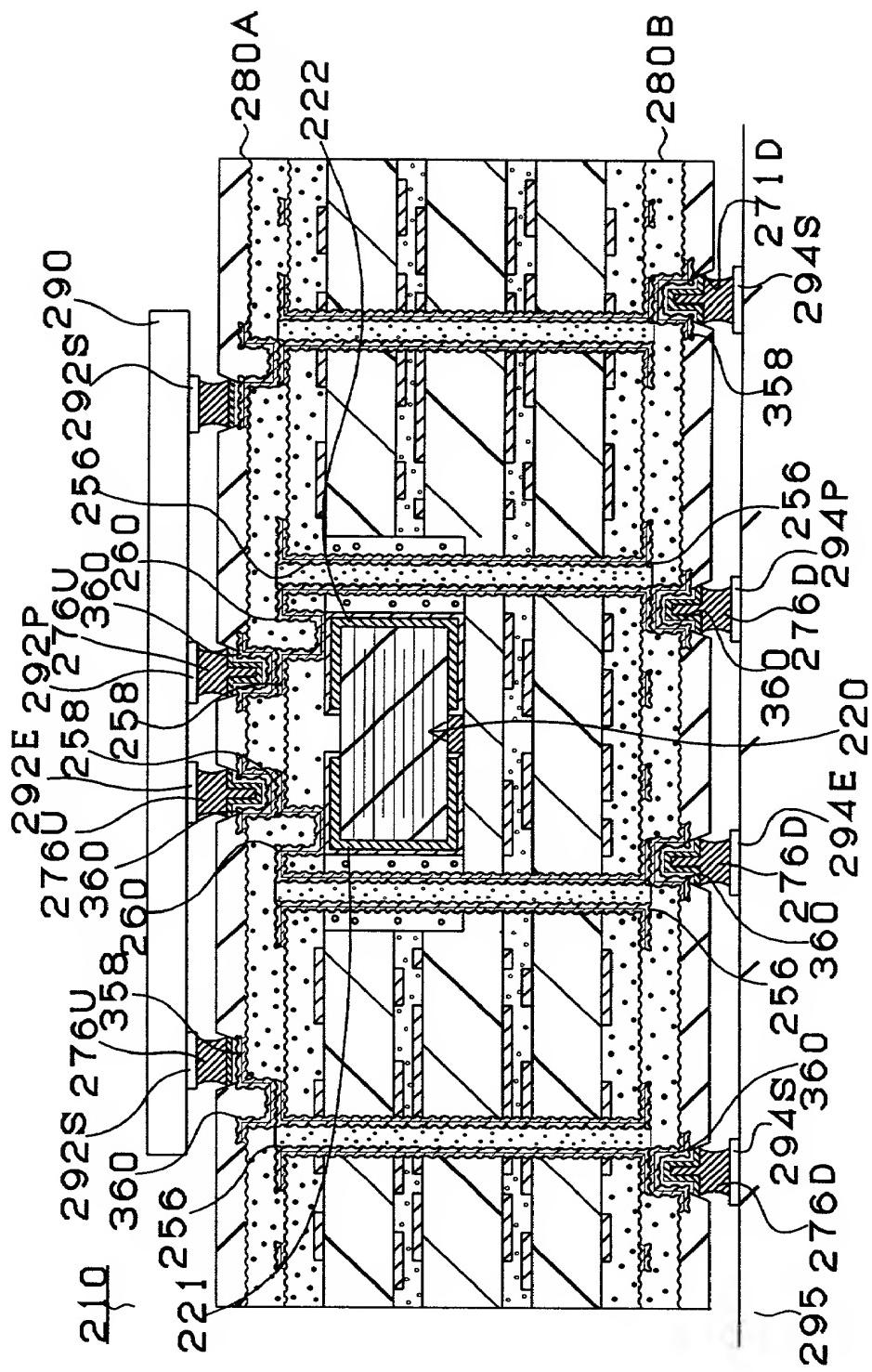
09/830360

19/53  
Fig. 19



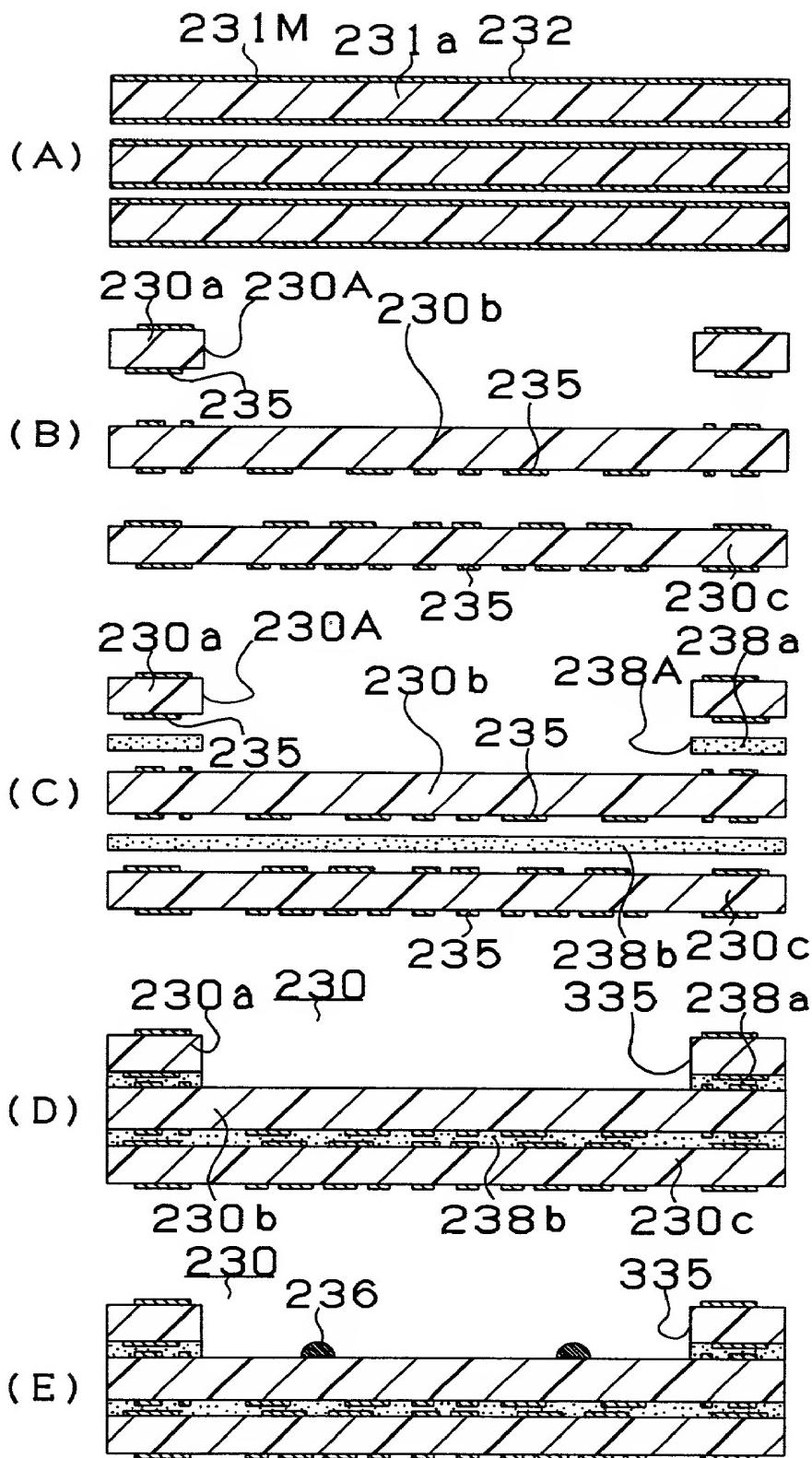
09/830360

20/53  
Fig. 20



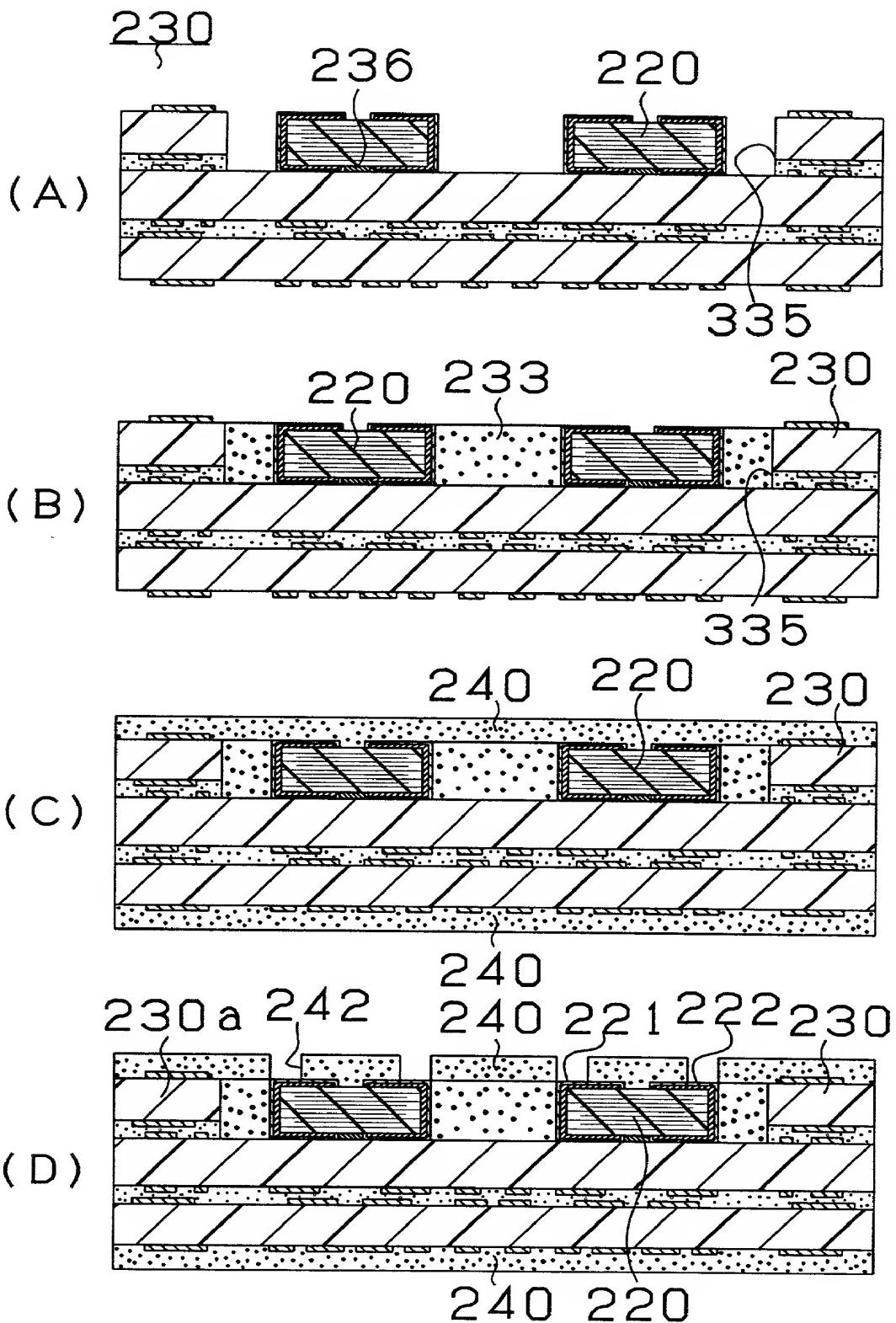
09/830360

21/53  
Fig. 21



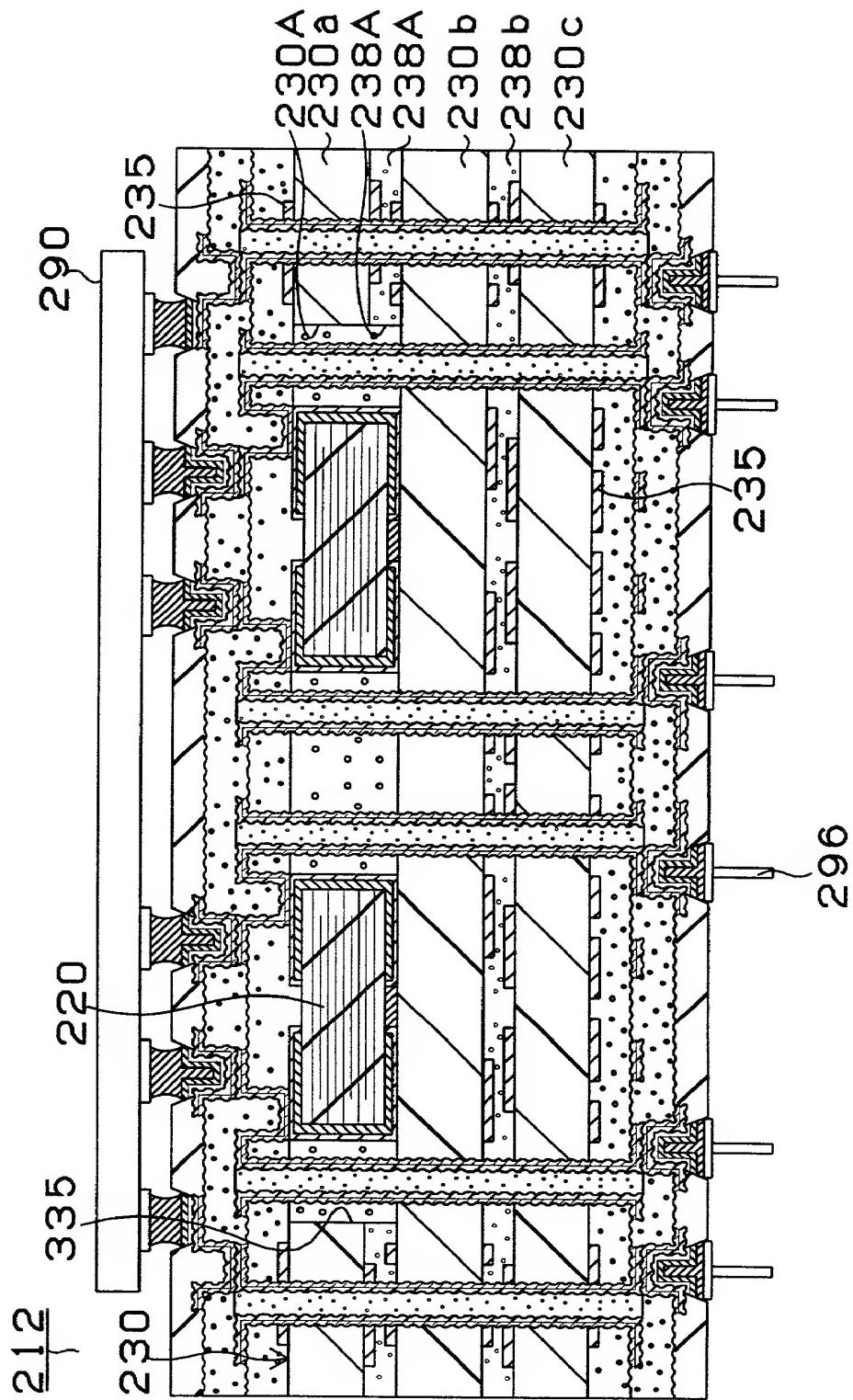
09/830360

22/53  
Fig. 22



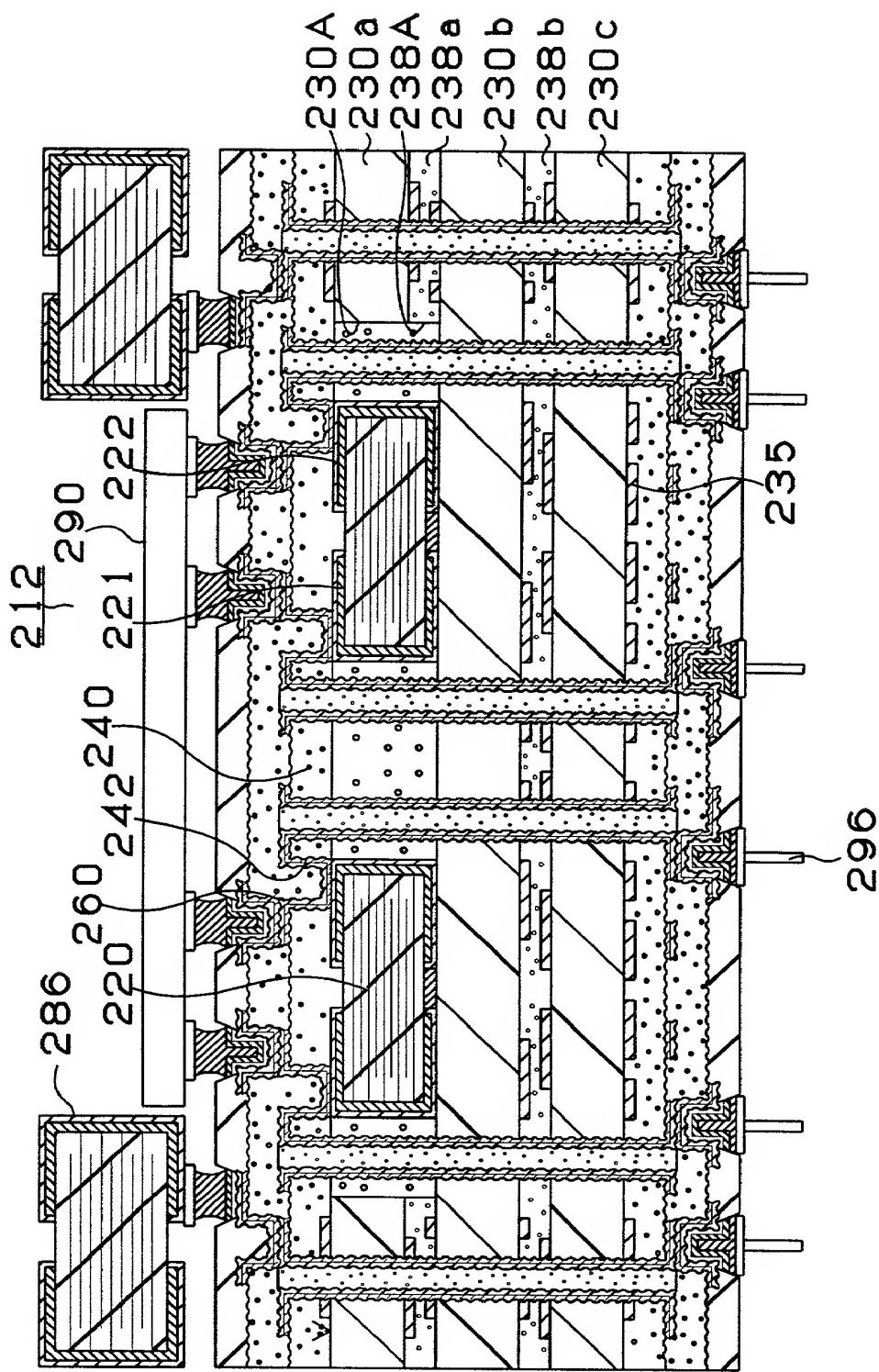
09/830360

Fig. 23  
23/53



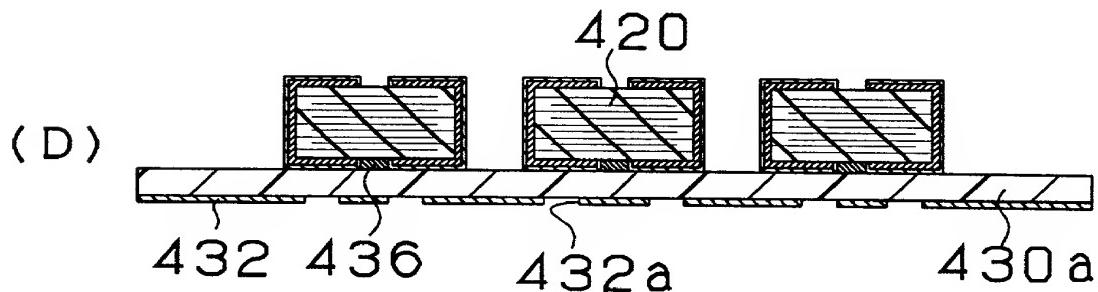
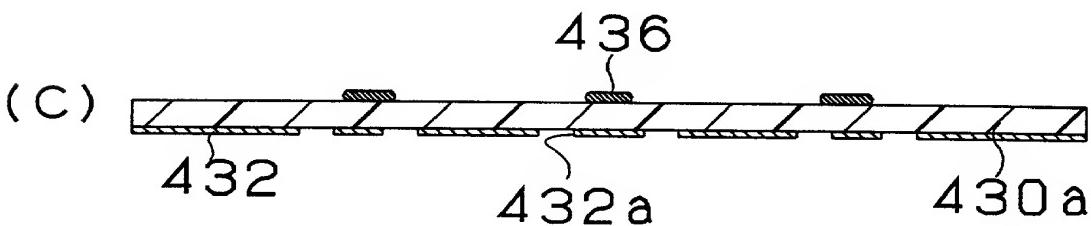
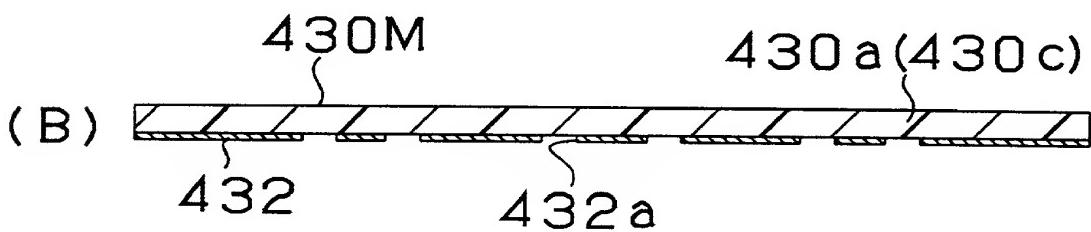
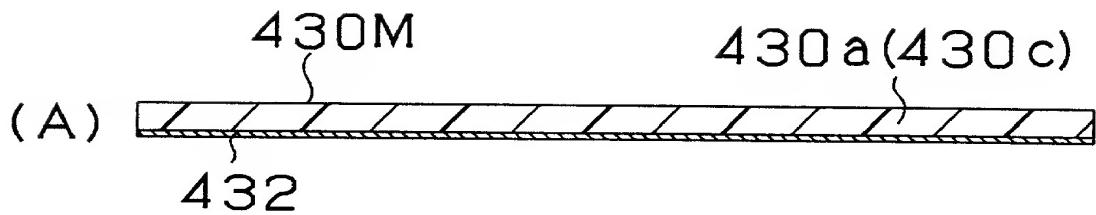
09/830360

24/53  
Fig. 24



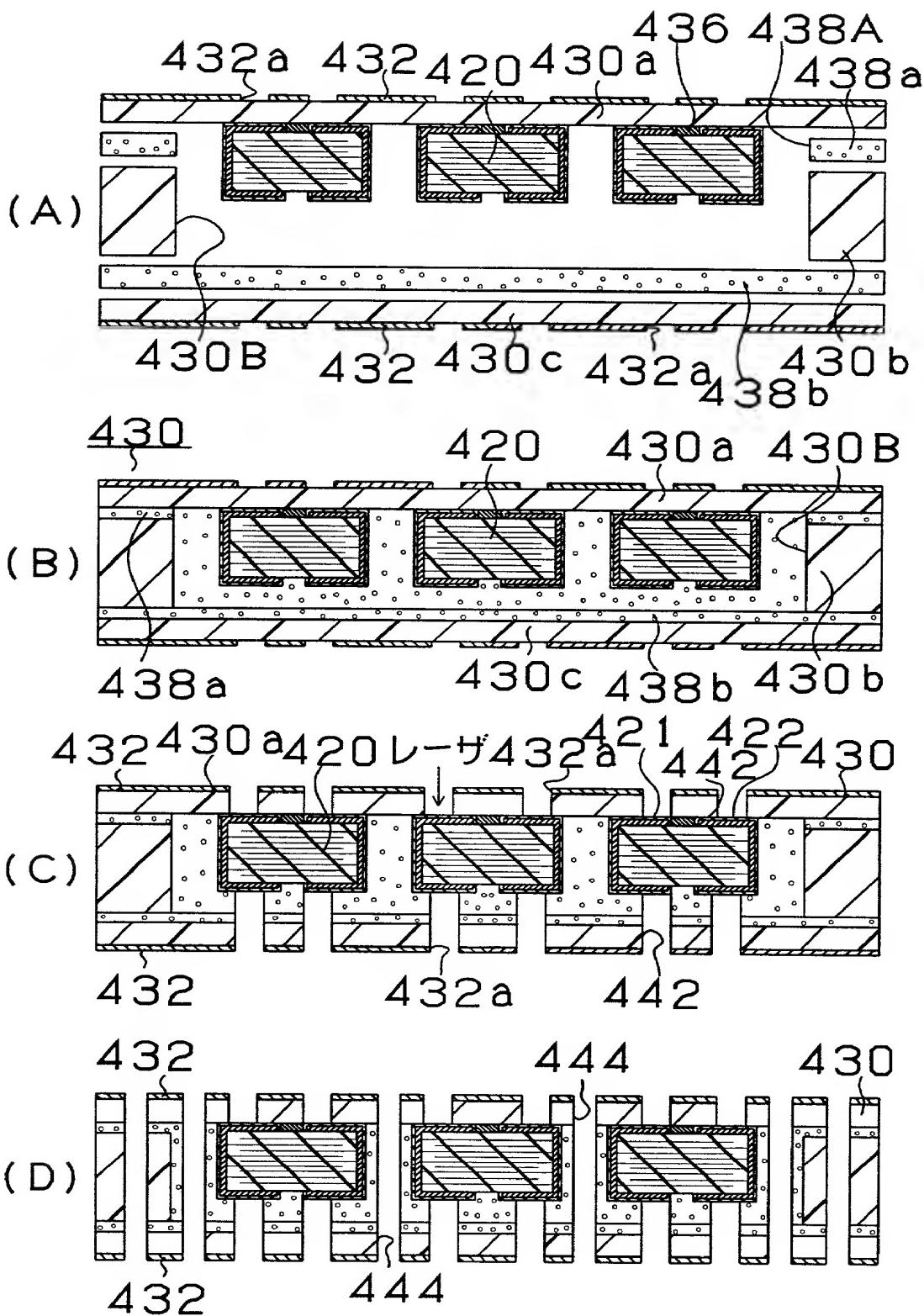
09/830360

25/53  
Fig. 25



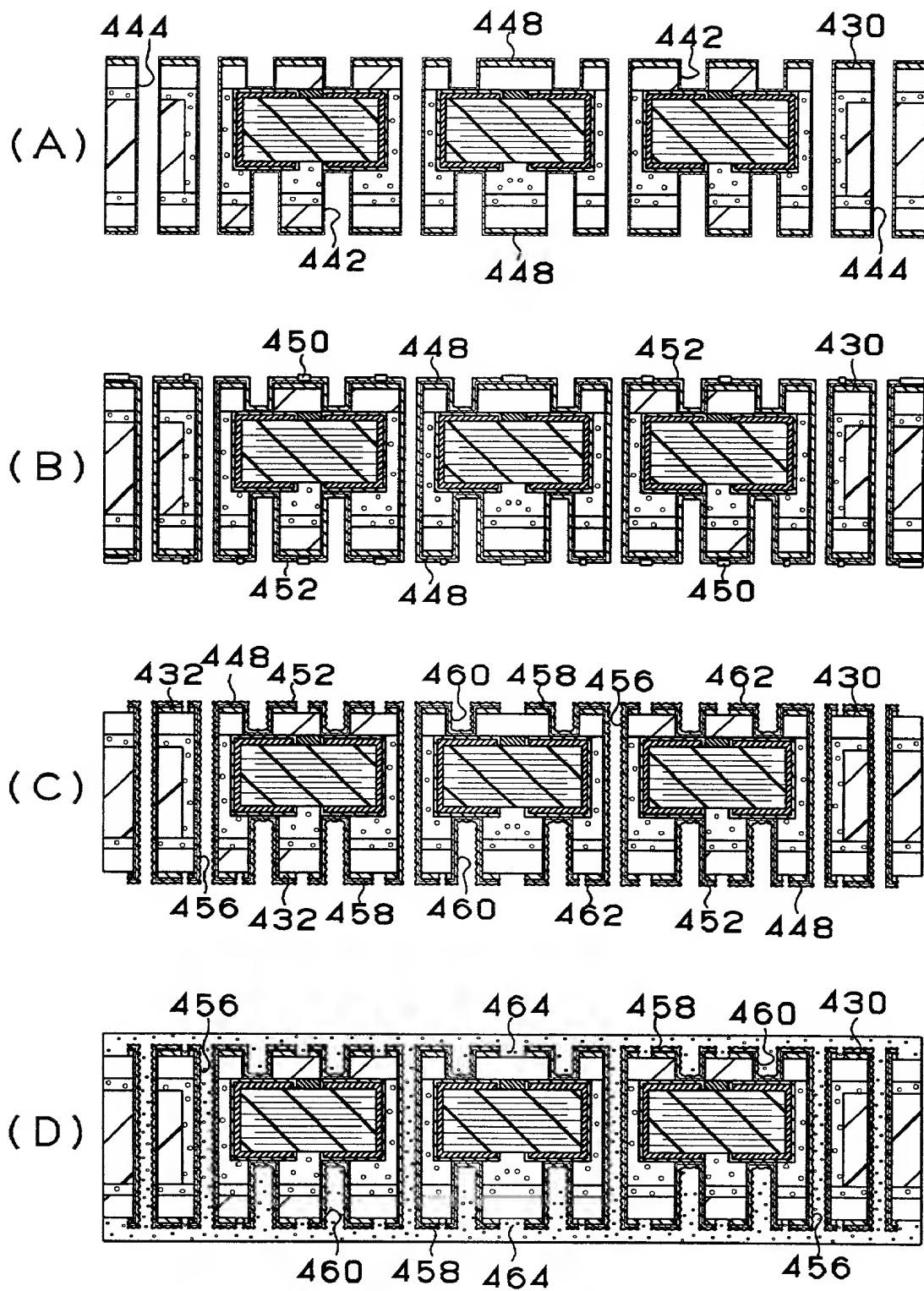
09/830360

26/53  
Fig. 26



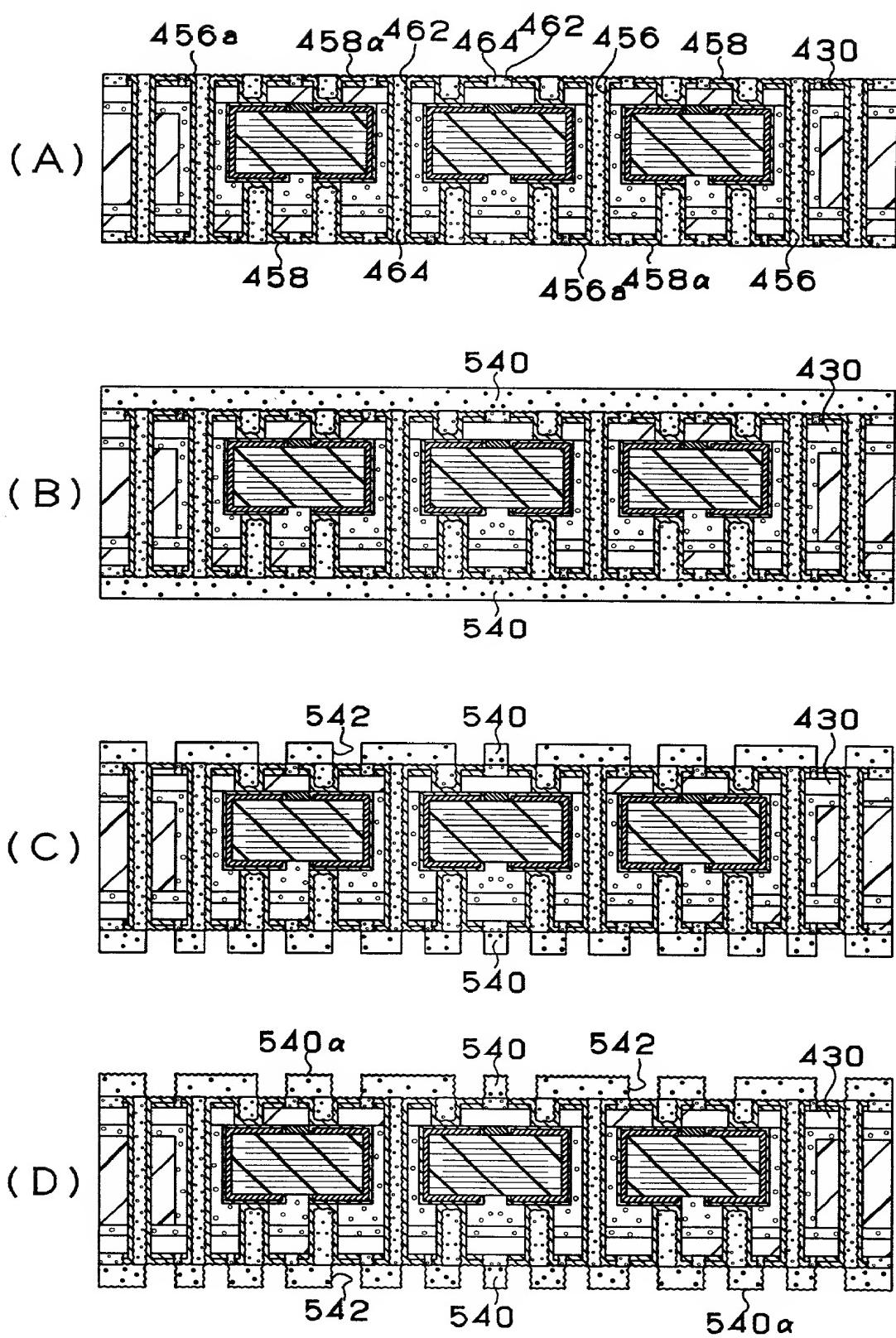
09/830360

27/53  
Fig. 27



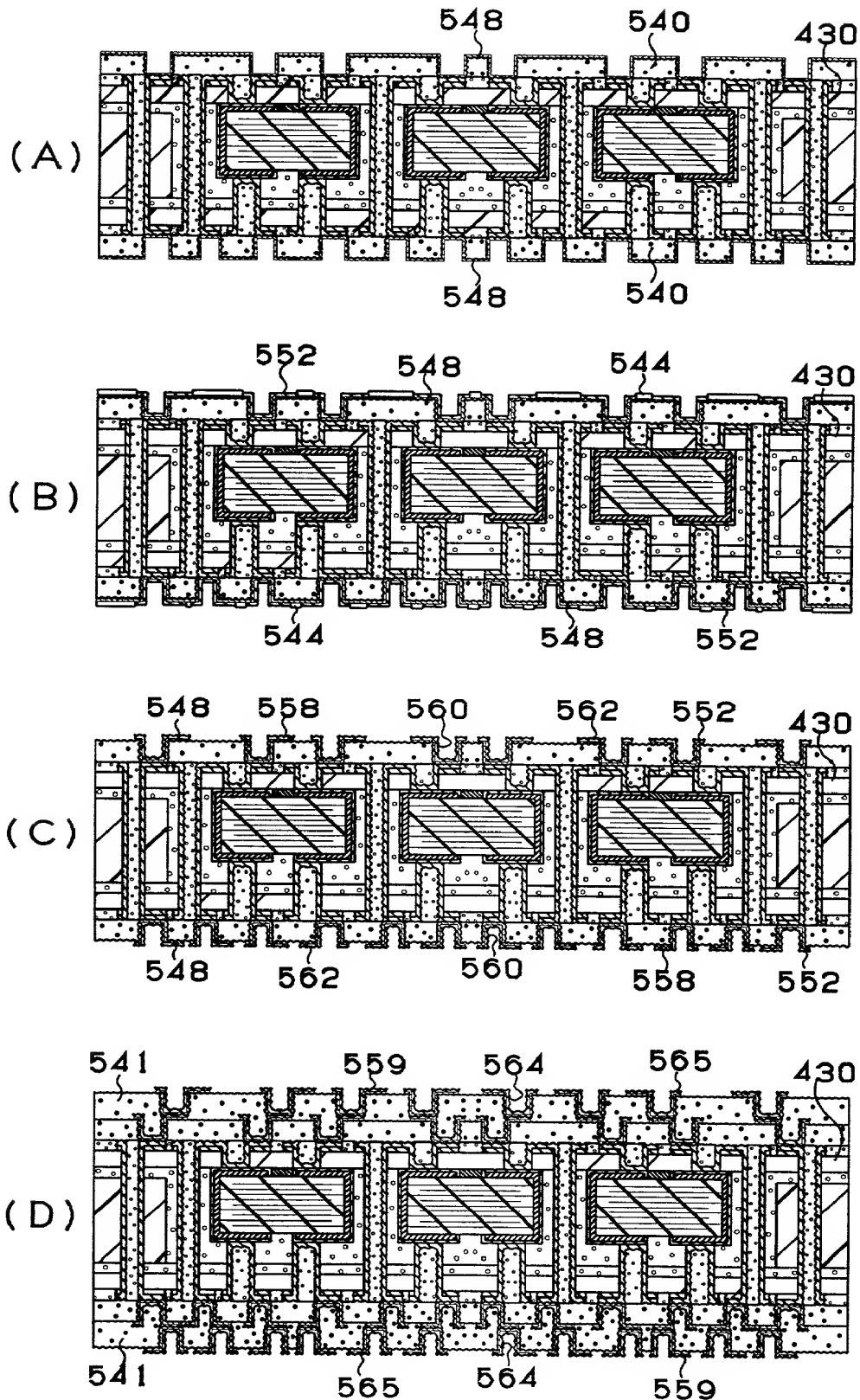
09/830360

28/53  
Fig. 28



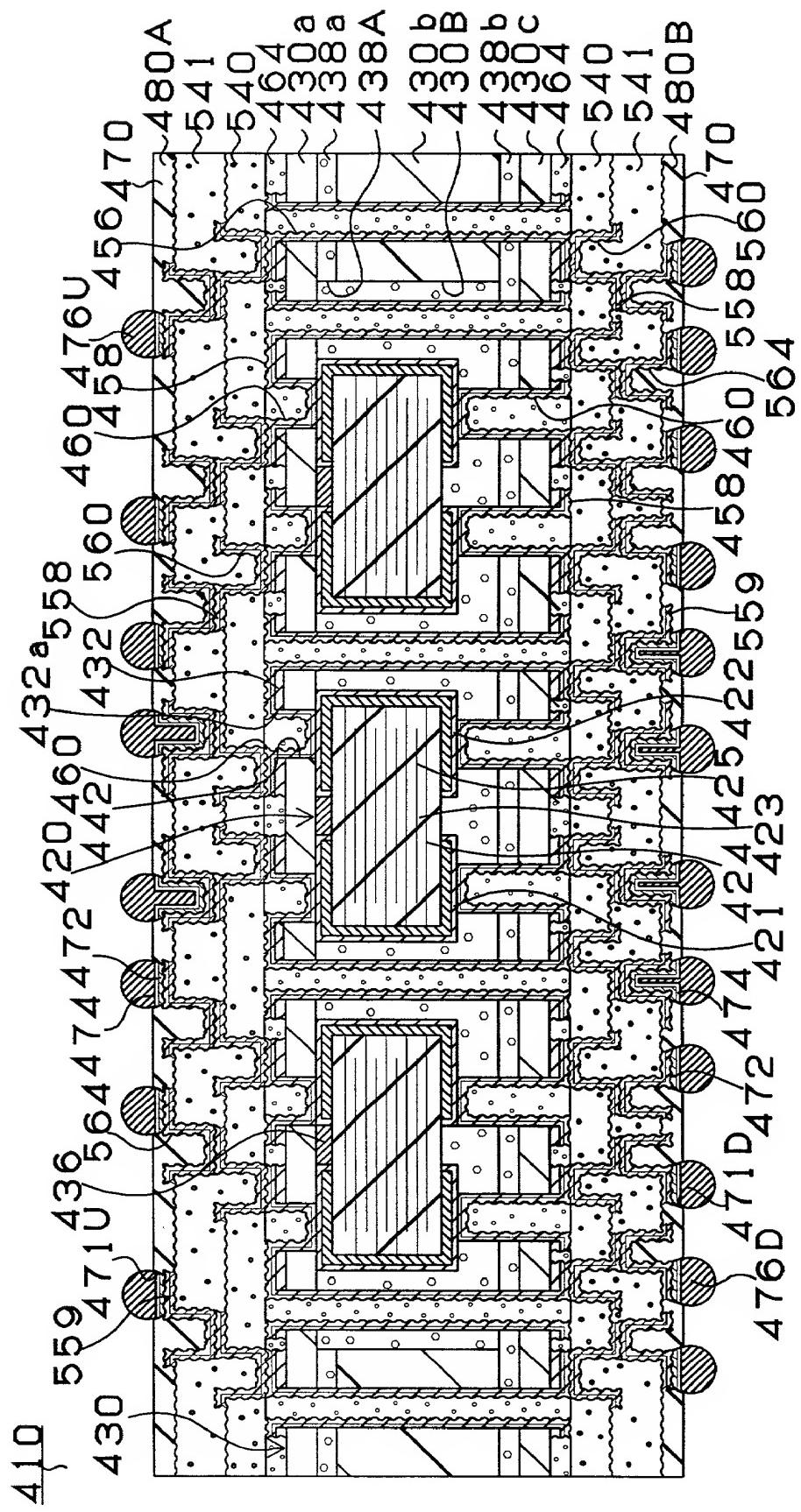
09/830360

29/53  
Fig. 29



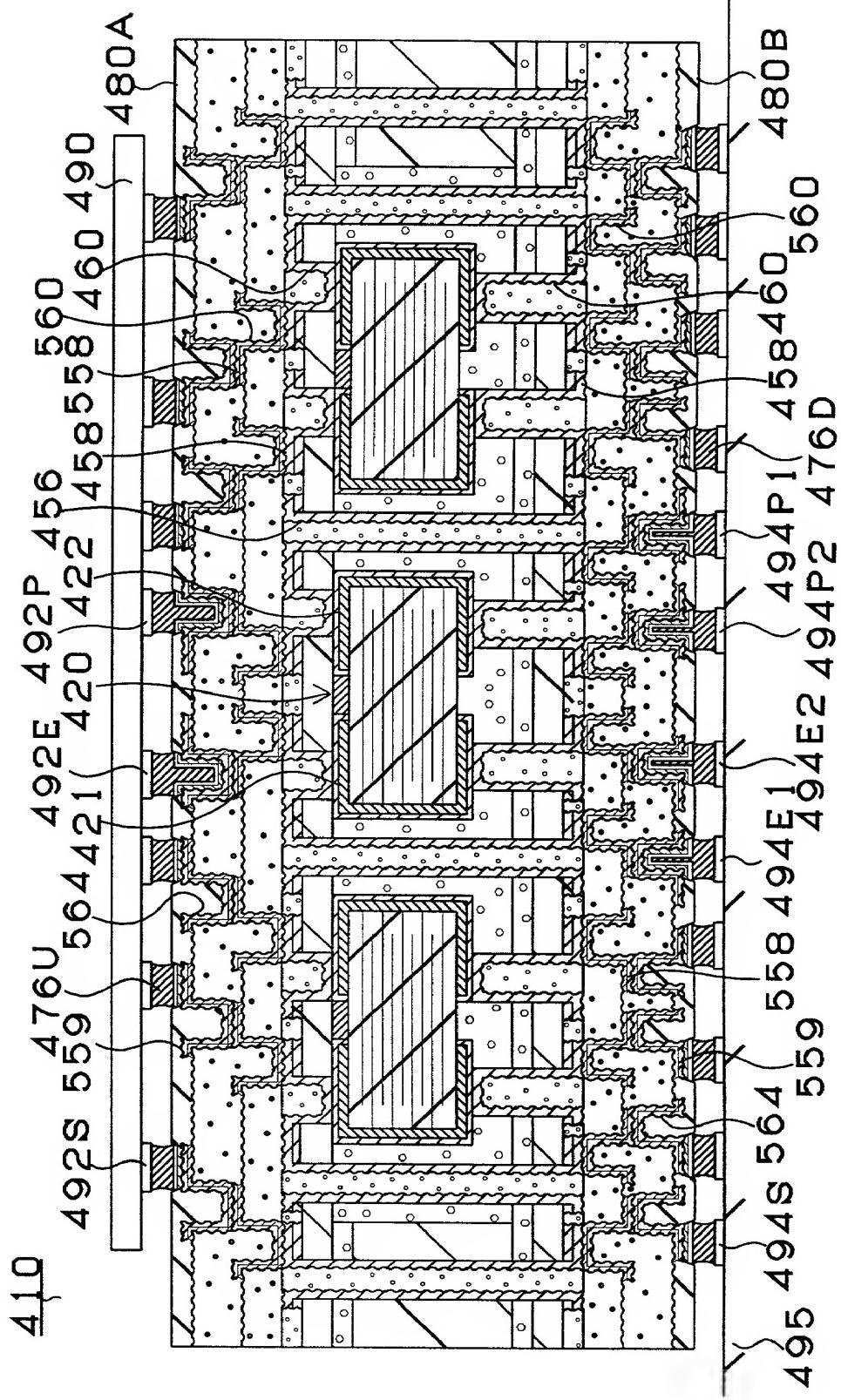
09/830360

Fig. 30  
30/53



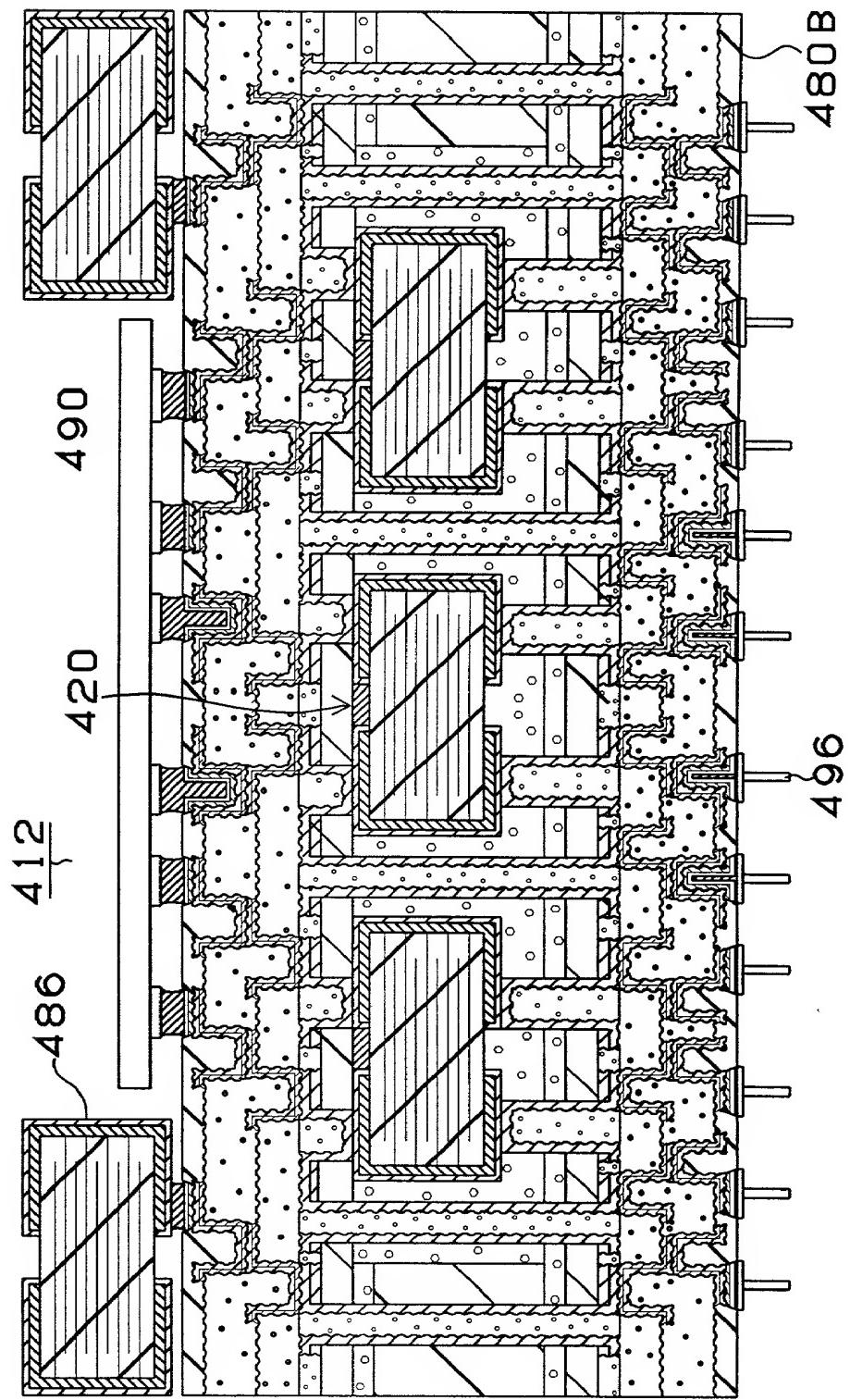
09/830360

31/53  
Fig. 31

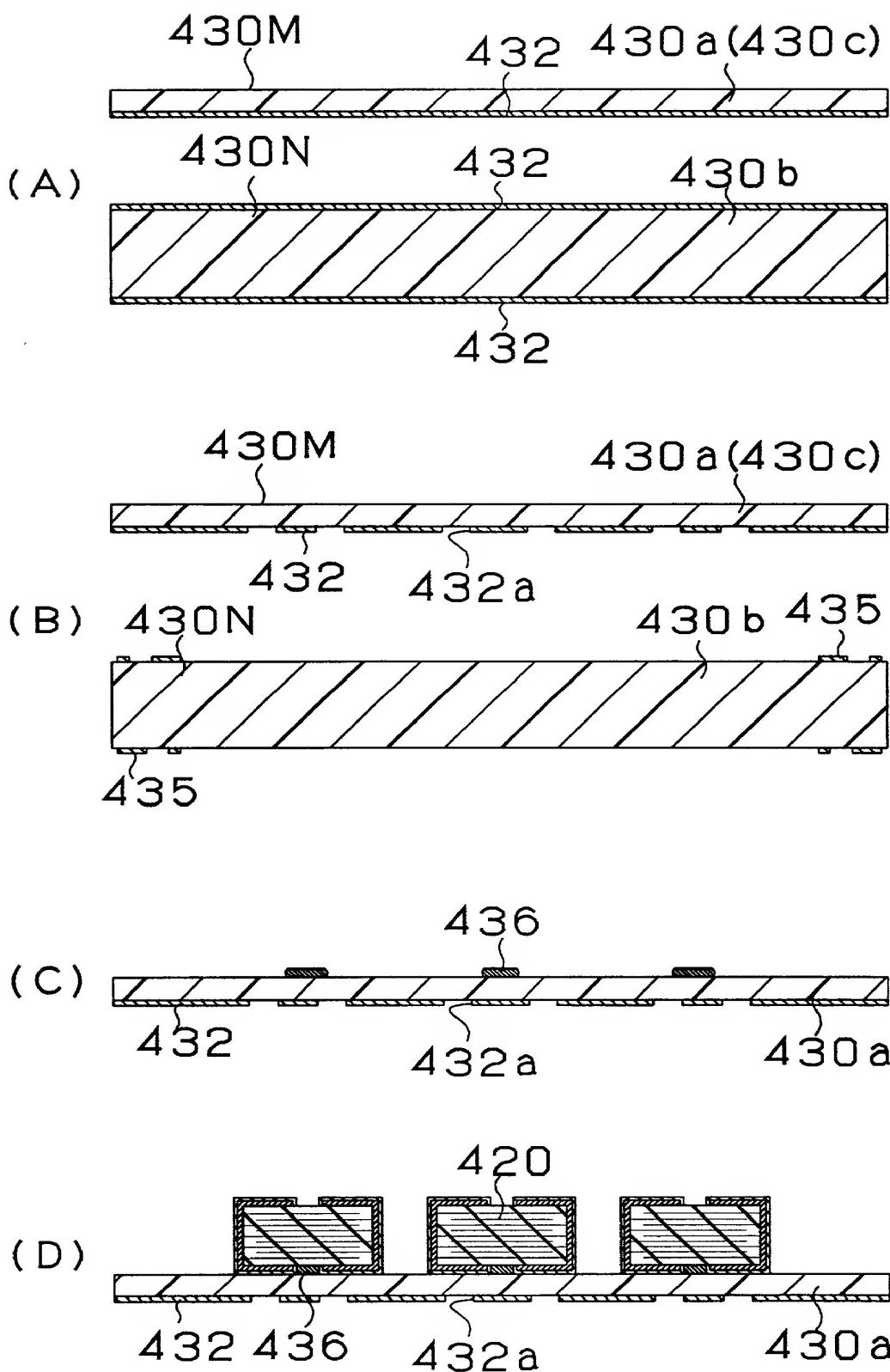


09/830360

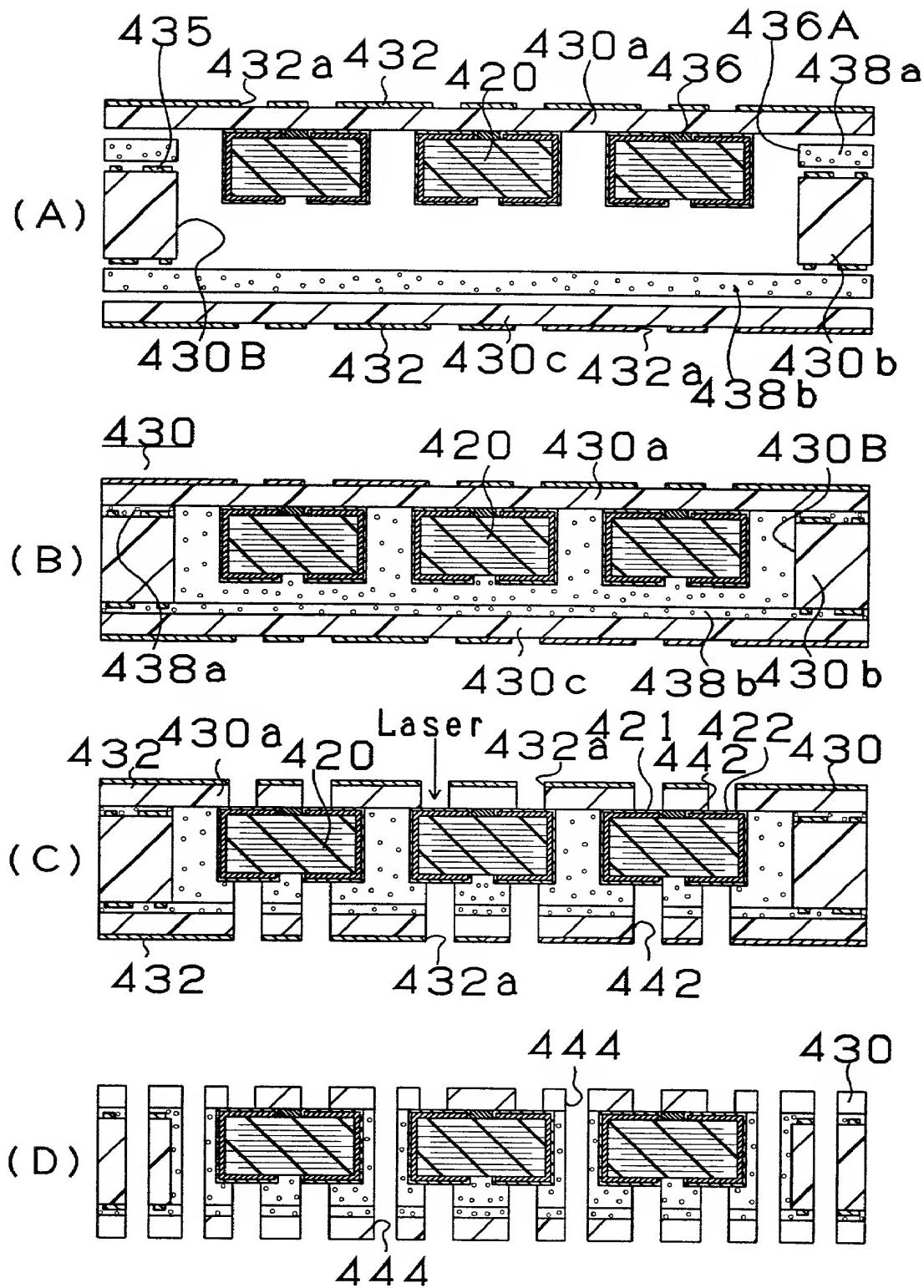
32/53  
Fig. 32



33/53  
Fig. 33

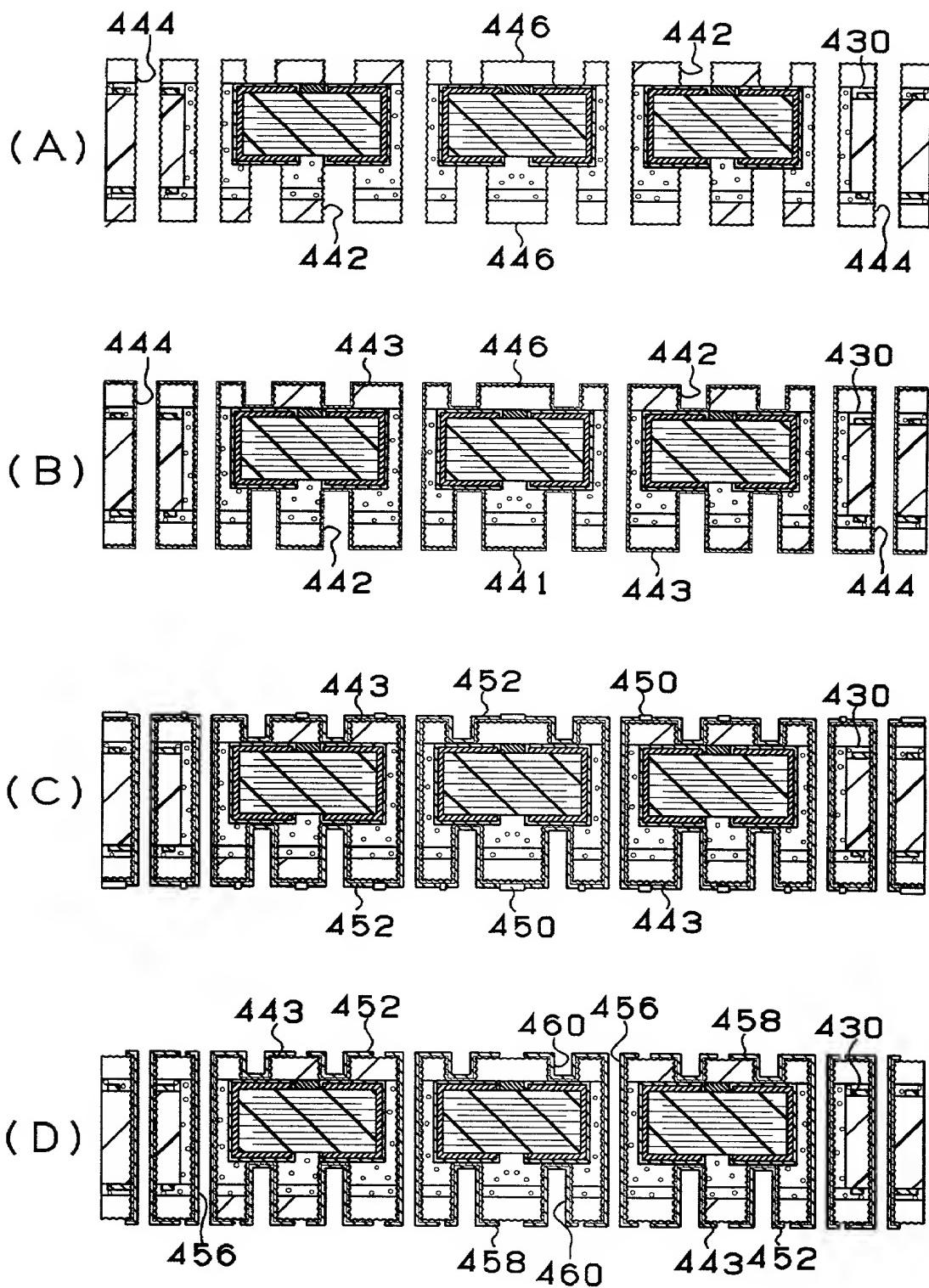


34/53  
Fig. 34



09/830360

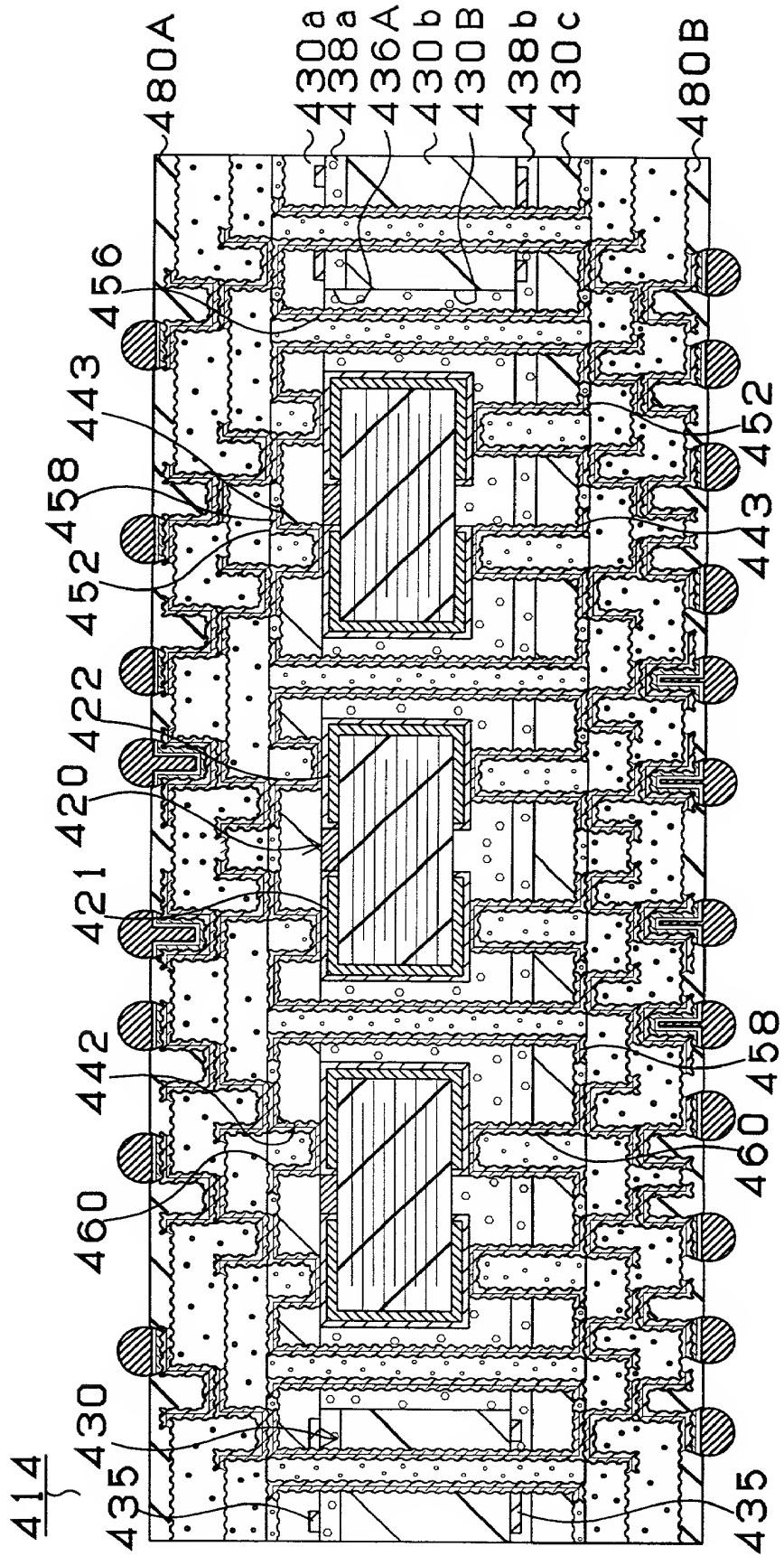
35/53  
Fig. 35

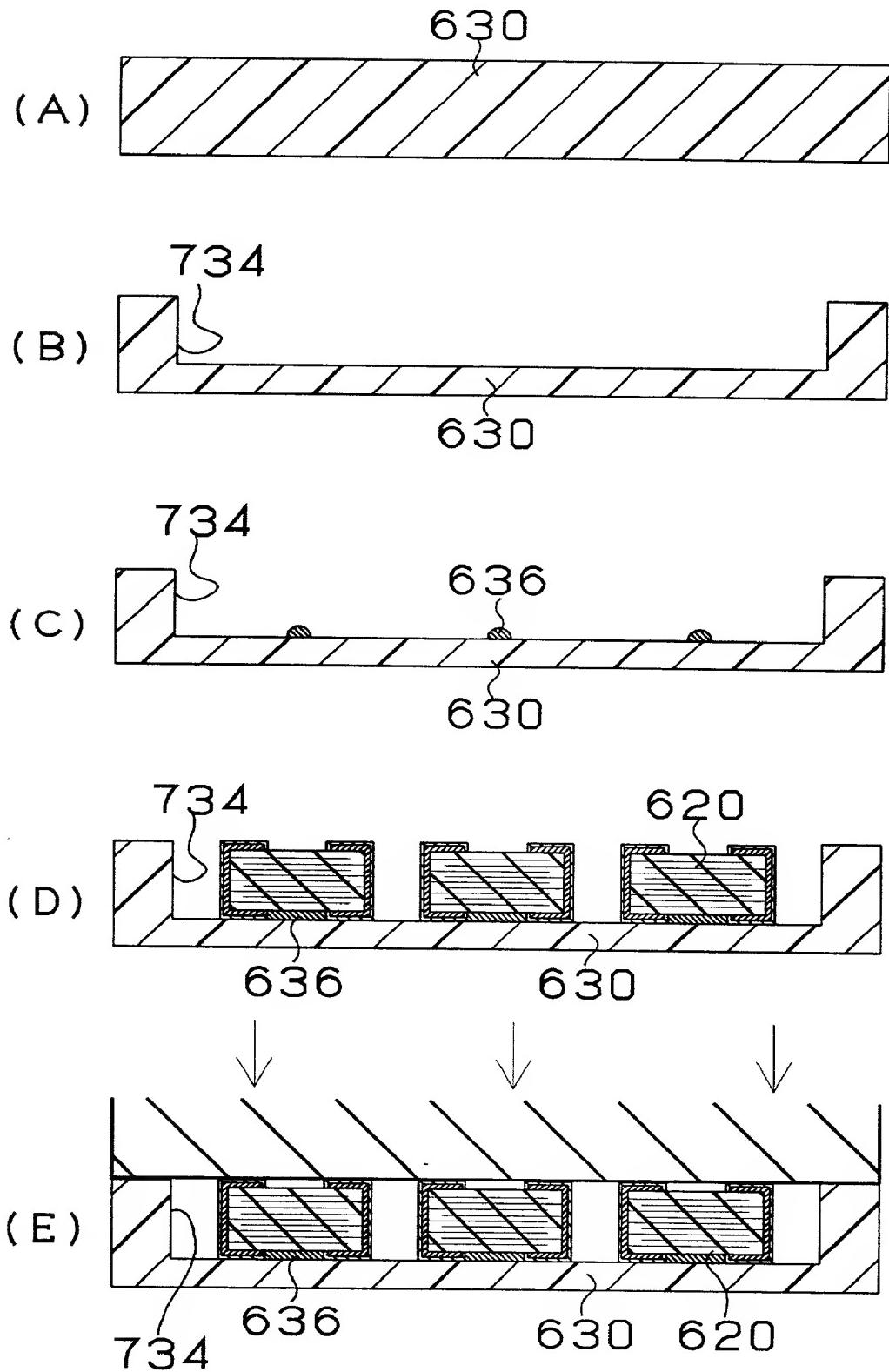


09/830360 - C14225104

09/830360

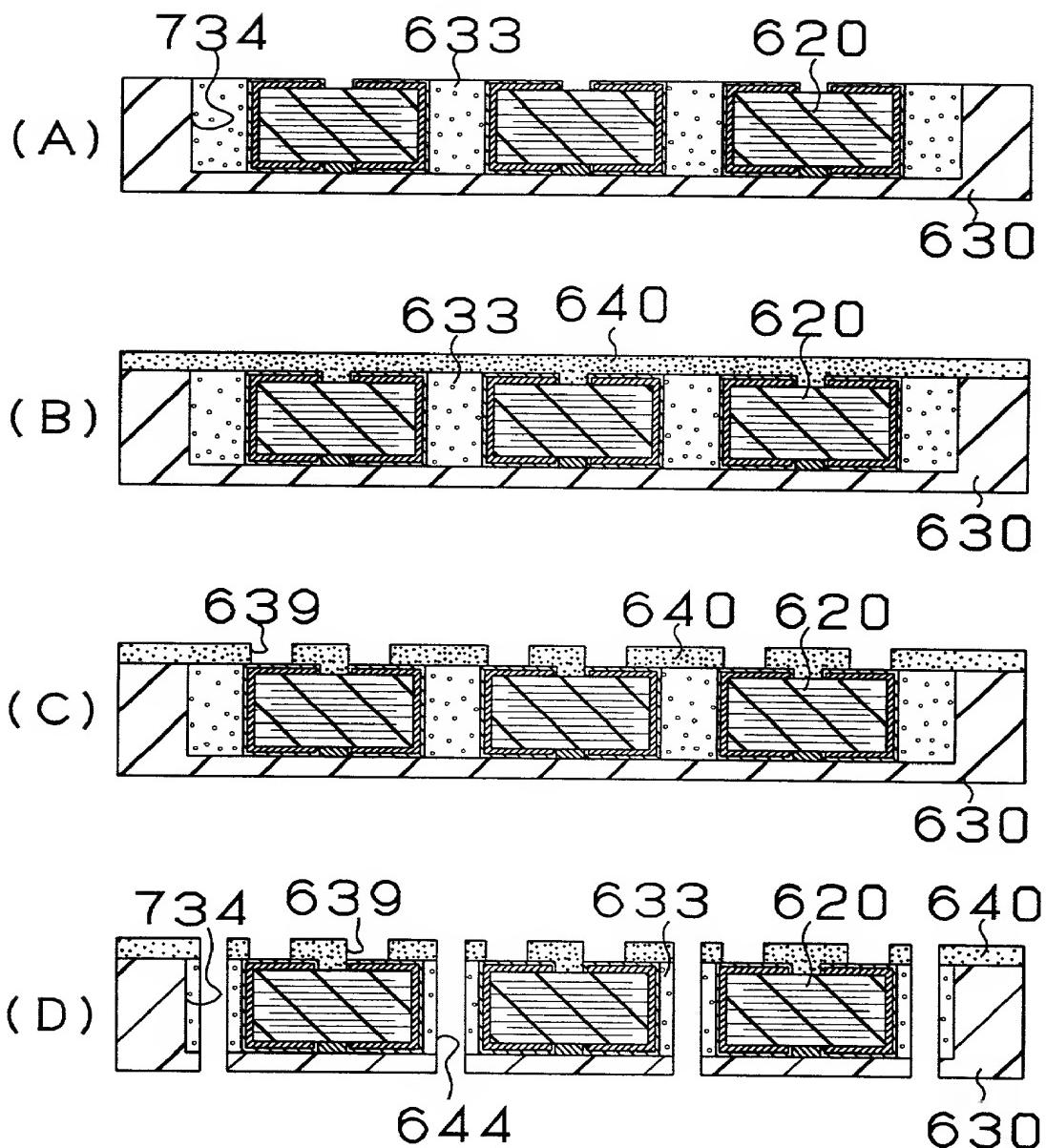
36/53  
Fig. 36



37/53  
Fig. 37

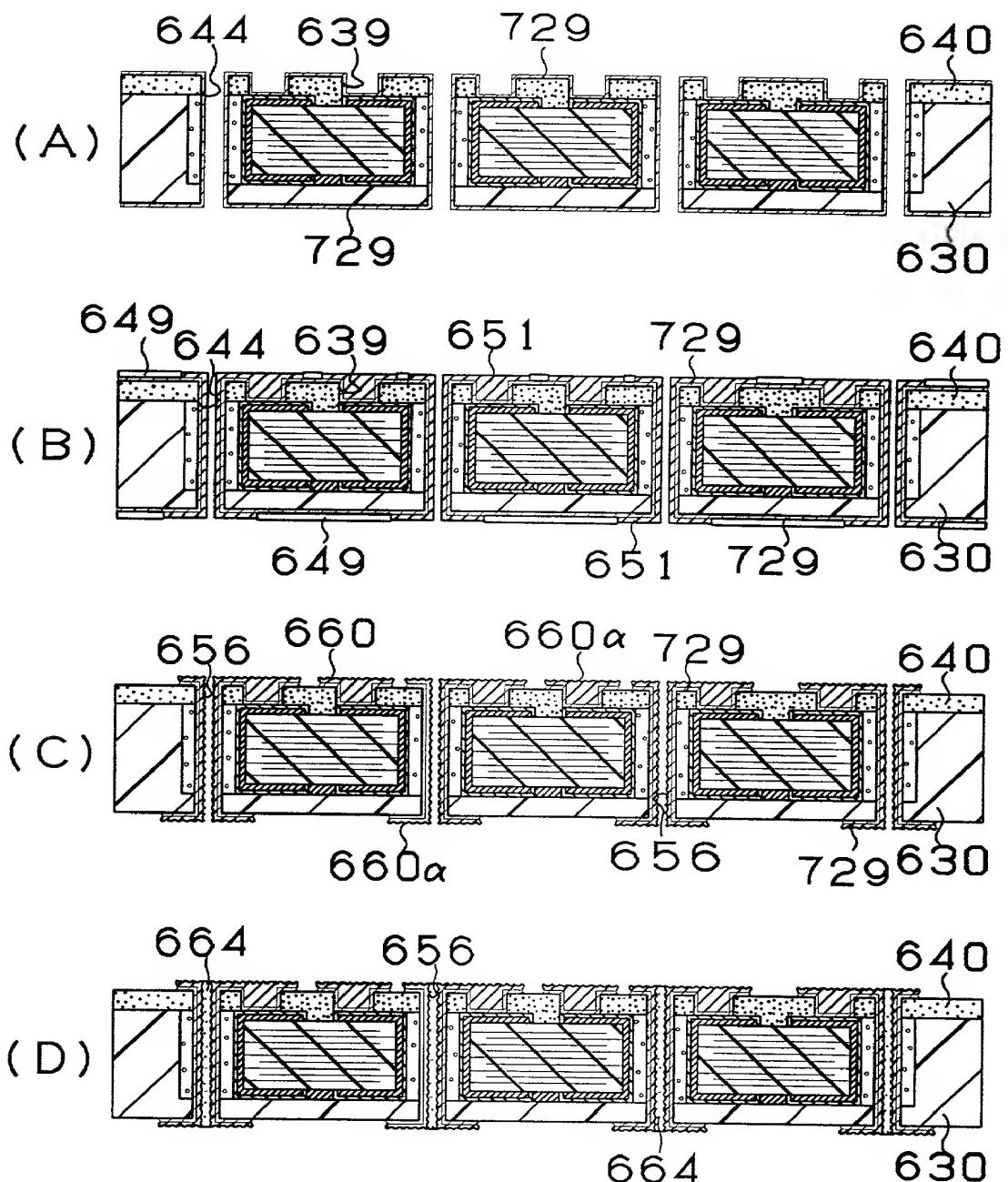
09/830360

38/53  
Fig. 38



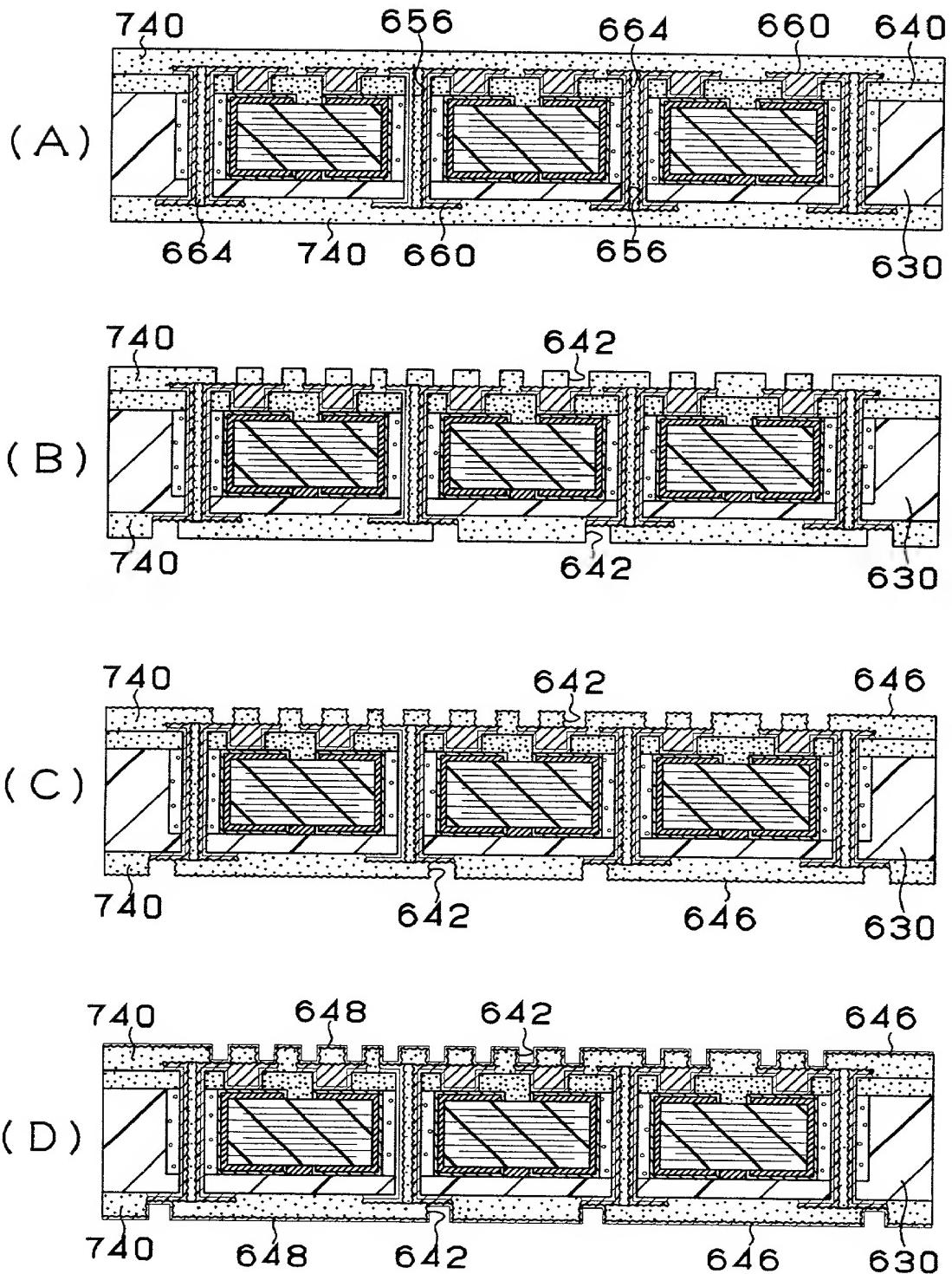
09/830360

39/53  
Fig. 39



09/830360

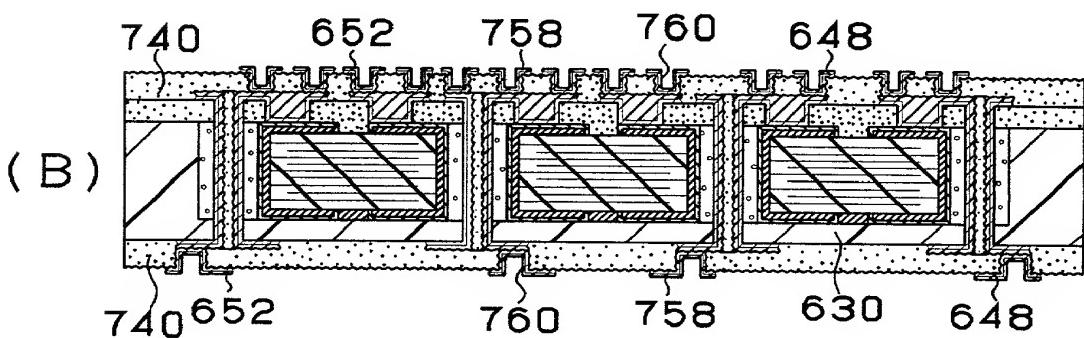
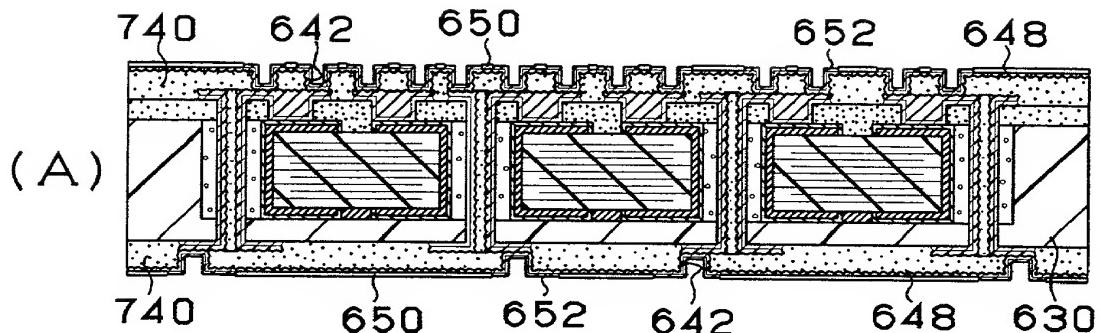
40/53  
Fig. 40



09/830360 - 31,250

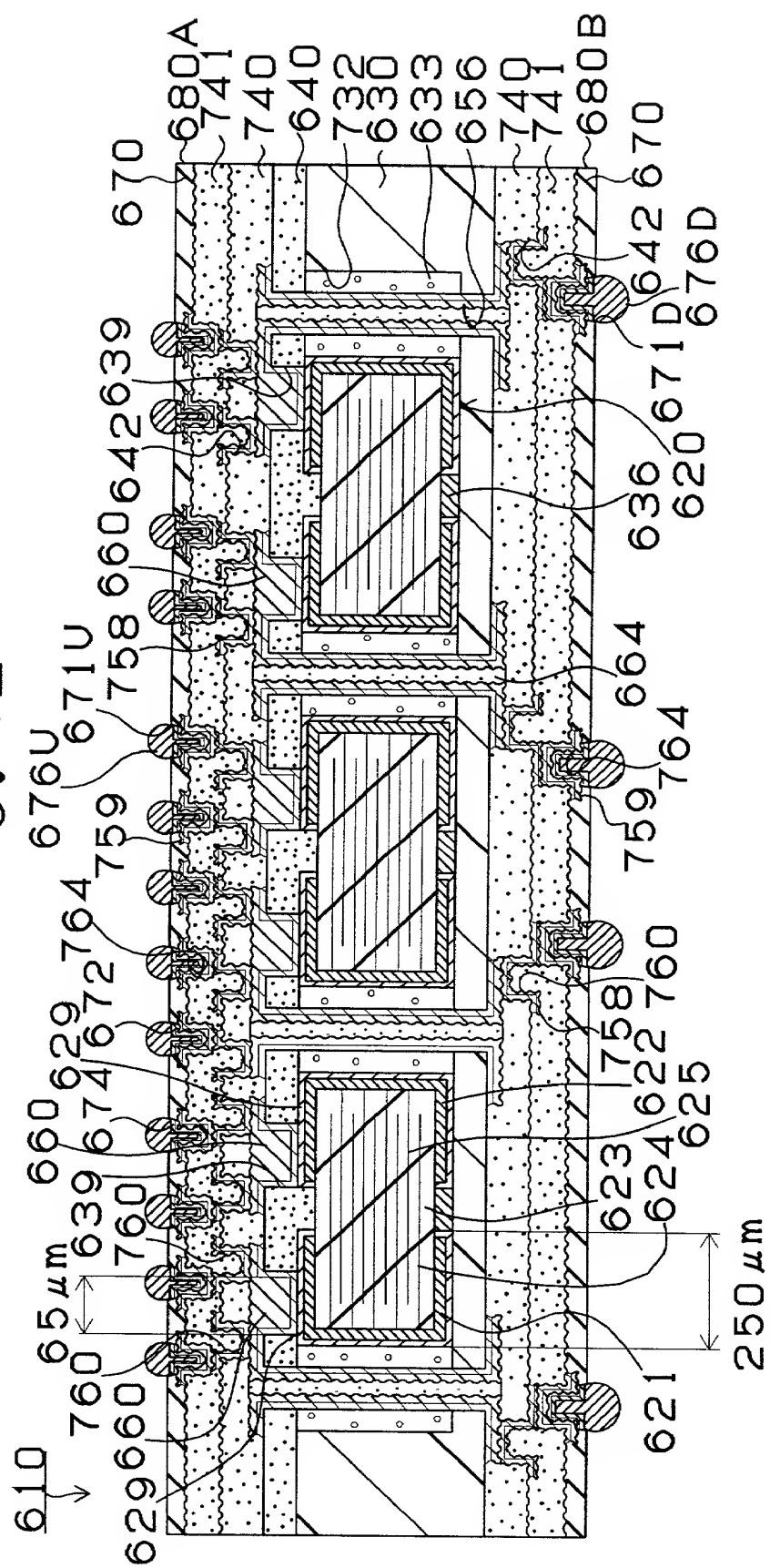
09/830360

41/53  
Fig. 41



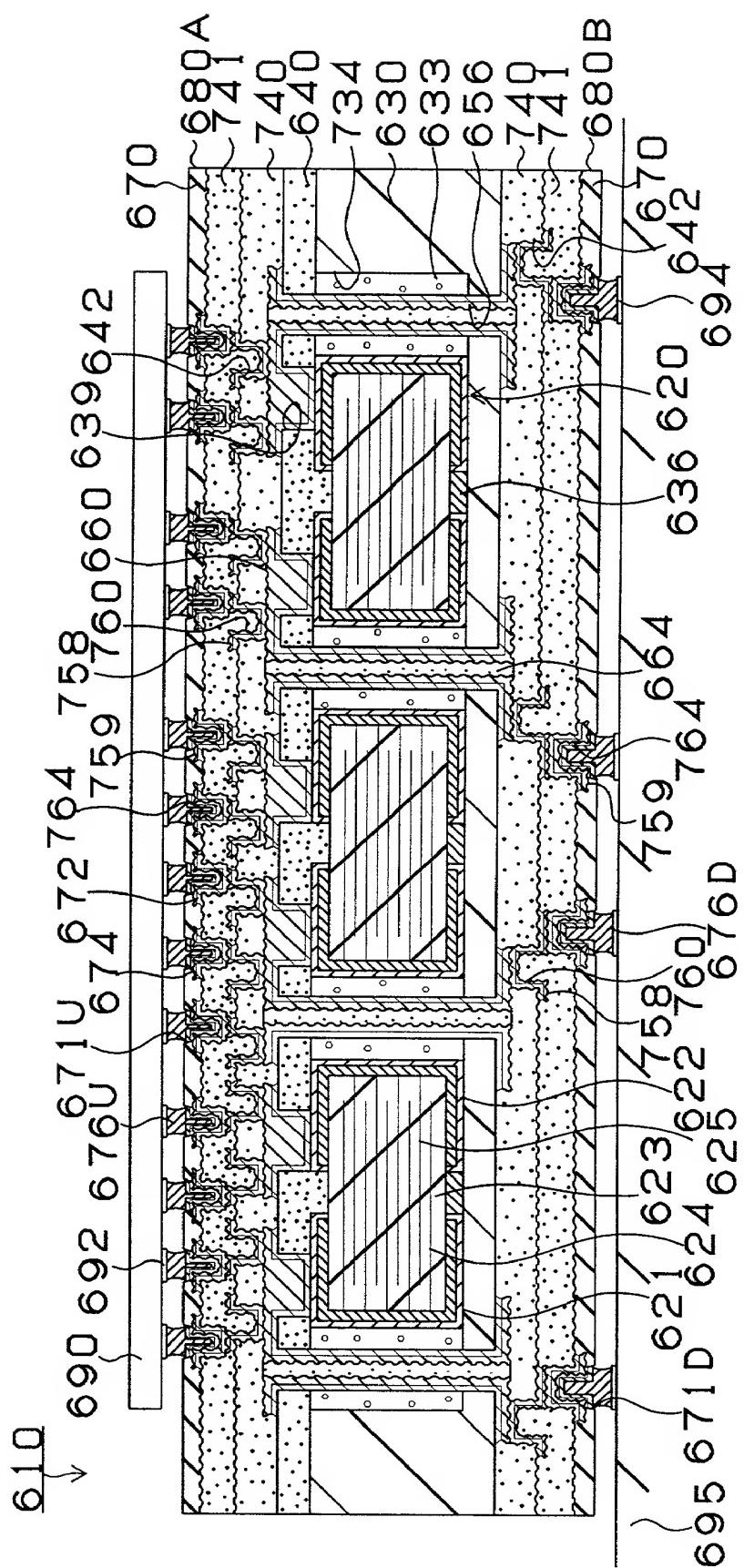
09/830360

42/53  
Fig. 42



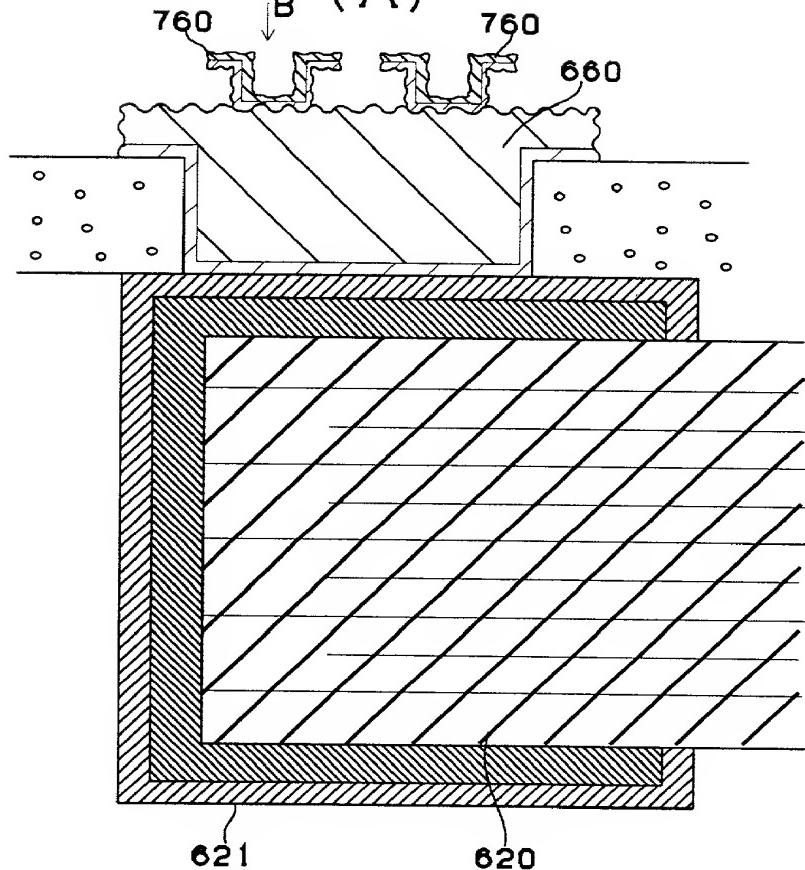
09/830360

43/53  
Fig. 43

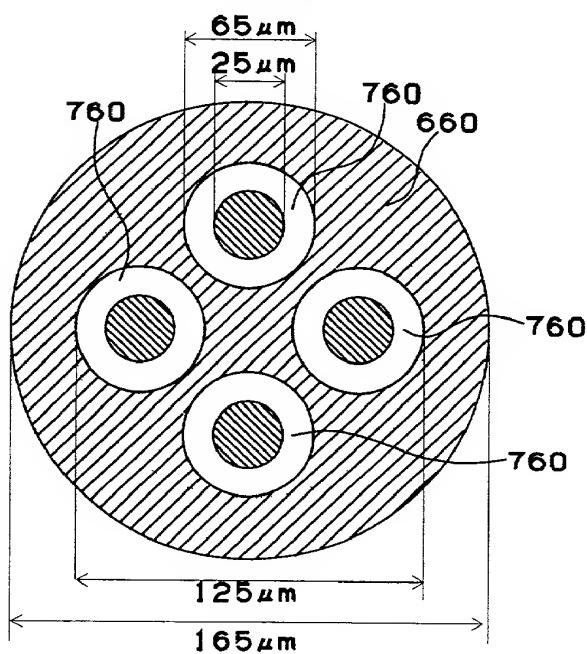


09/830360

44/53  
Fig. 44  
(A)

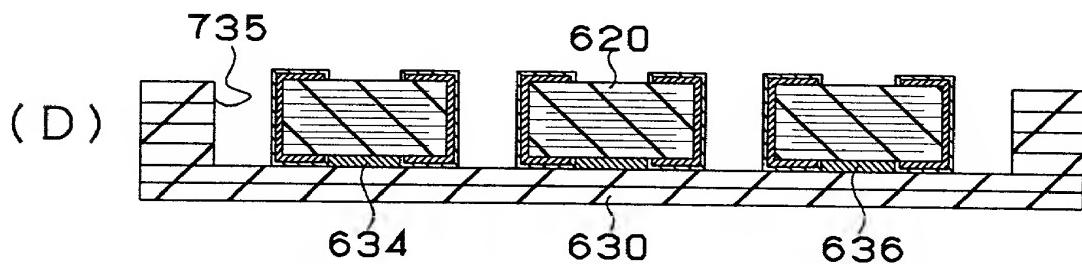
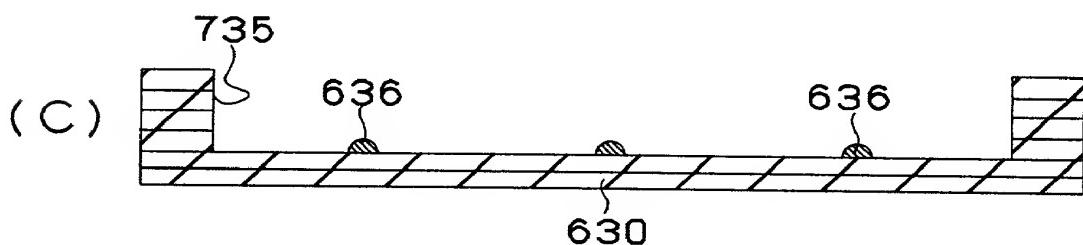
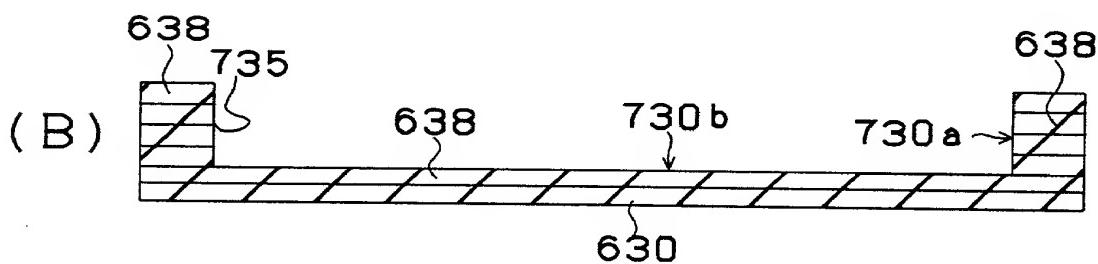
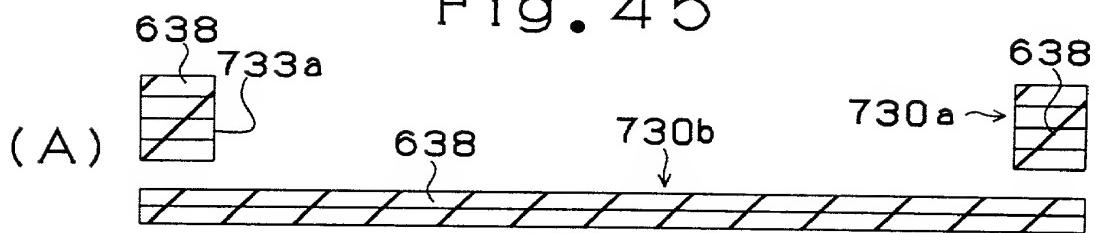


(B)



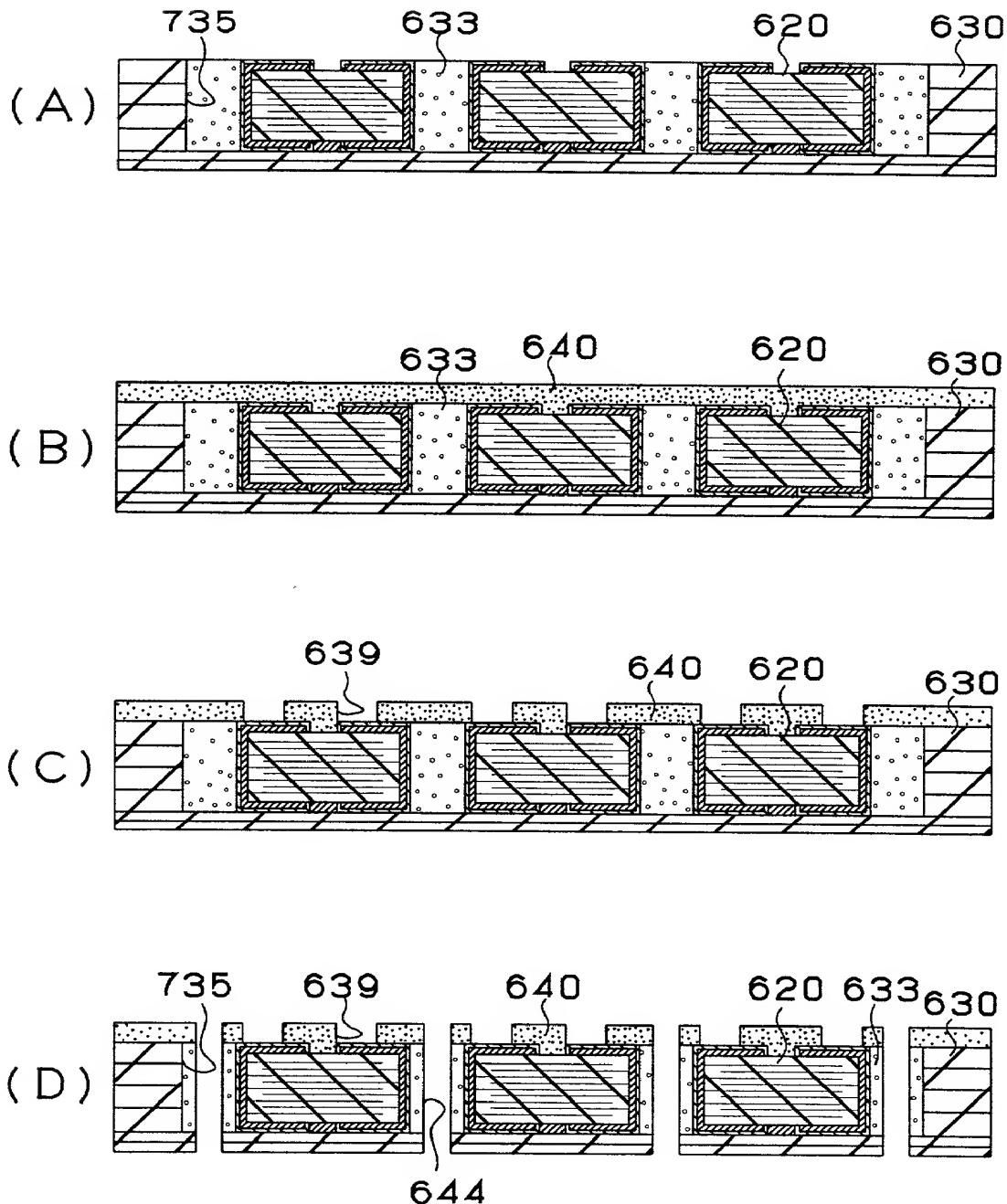
09/830360

45/53  
Fig. 45



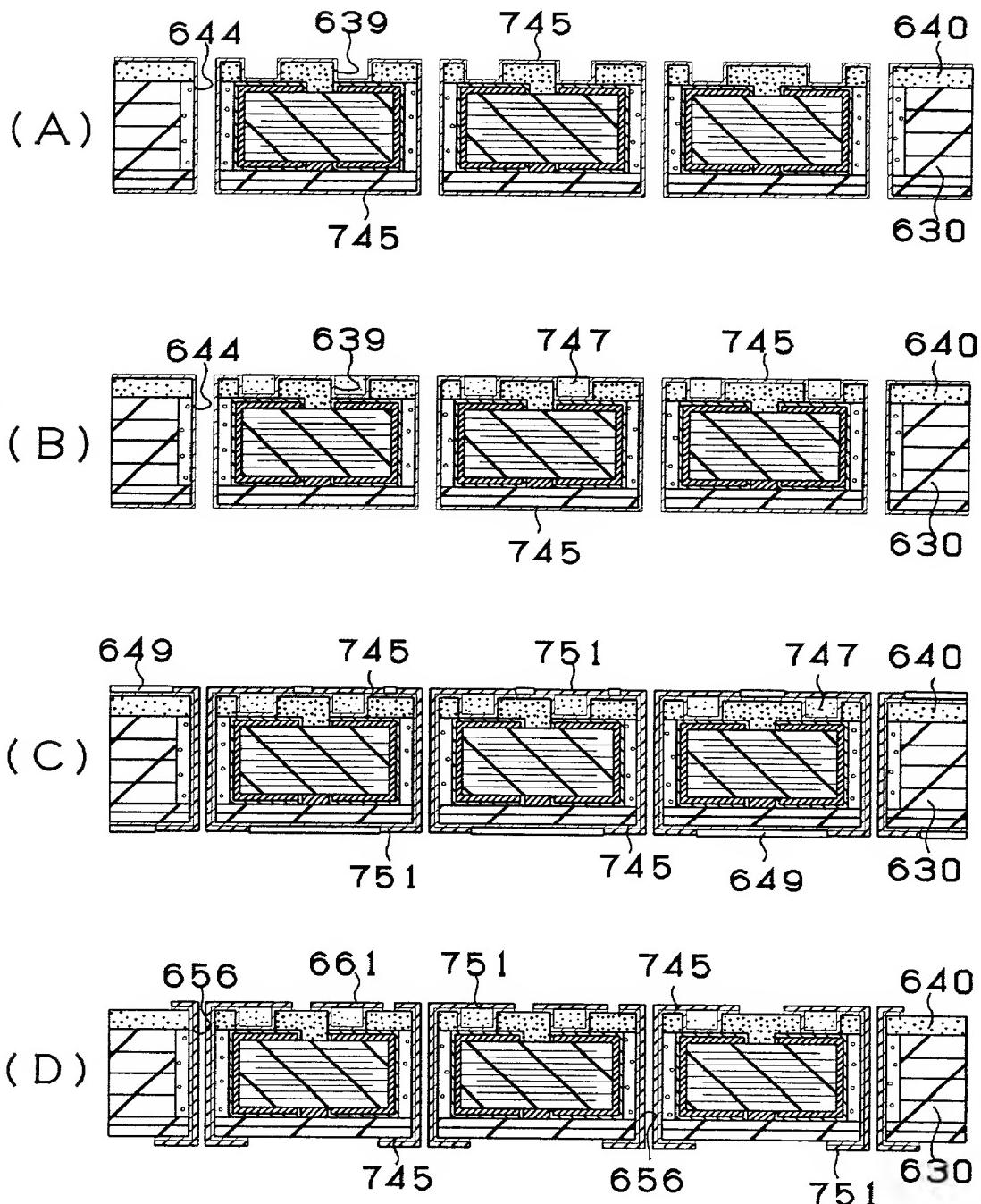
09/830360

46/53  
Fig. 46

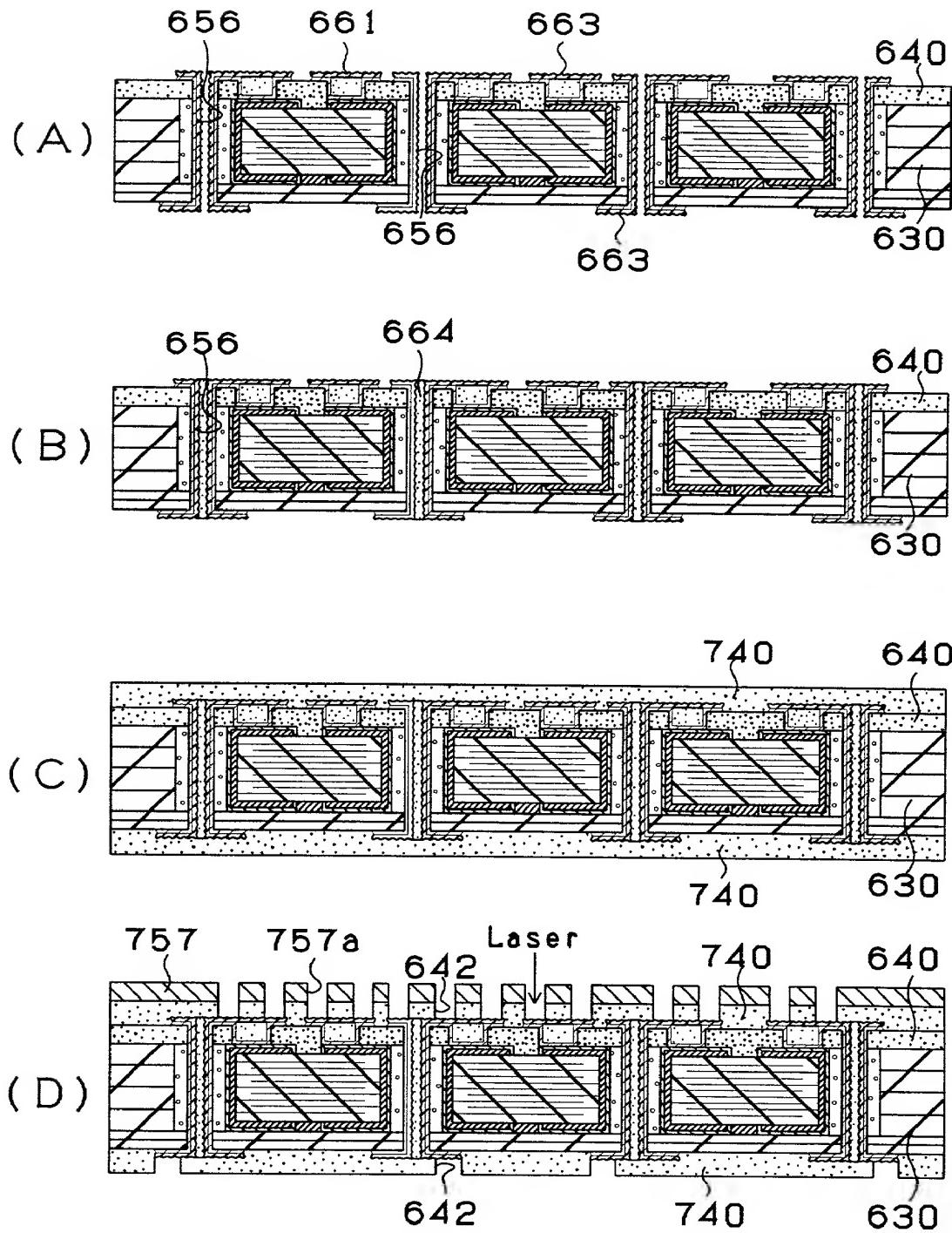


09/830360

47/53  
Fig. 47



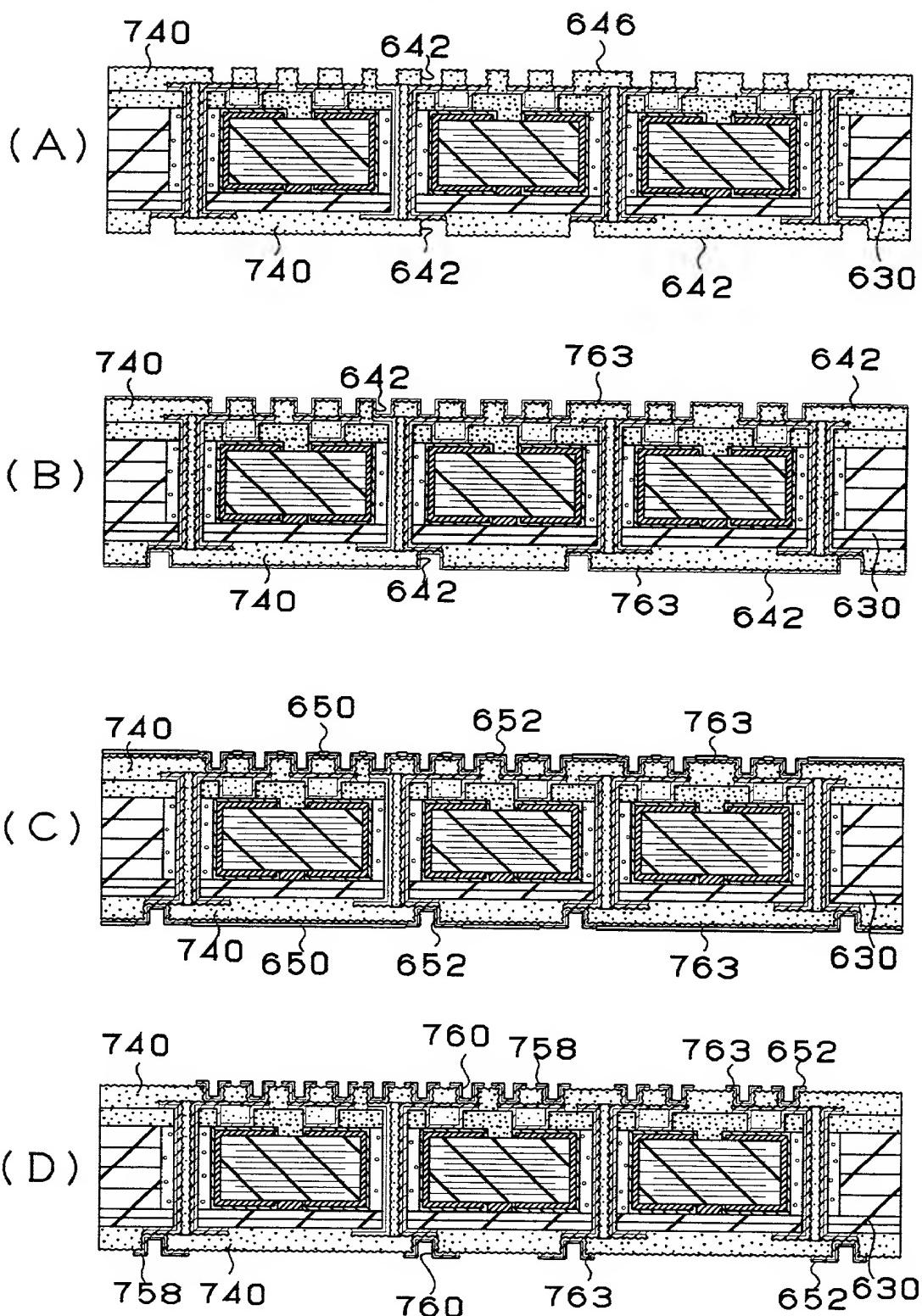
<sup>48/53</sup>  
Fig. 48



09/830360 - 3 of 25 pages

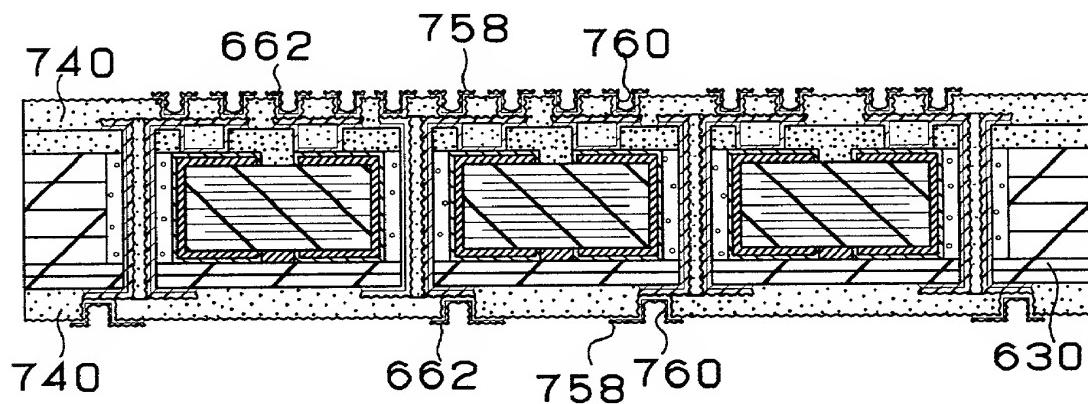
09/830360

49/53  
Fig. 49

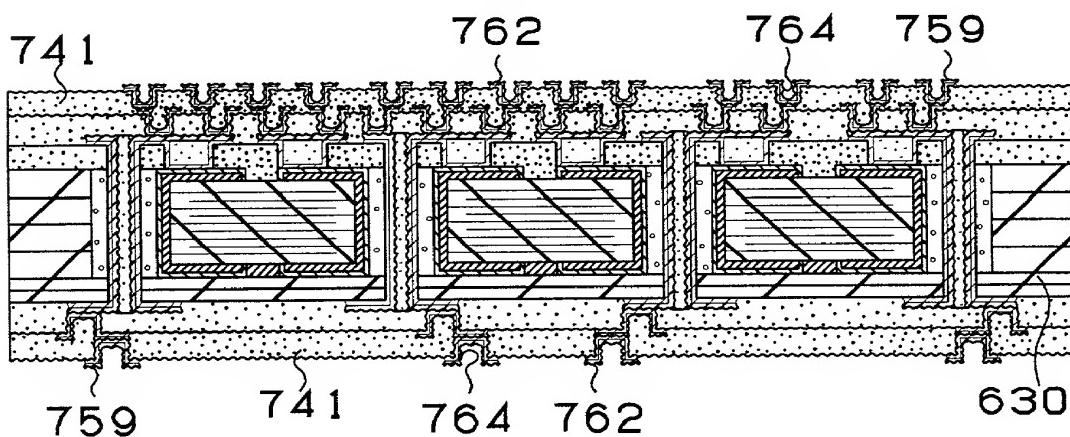


09/830360

50/53  
Fig. 50  
(A)



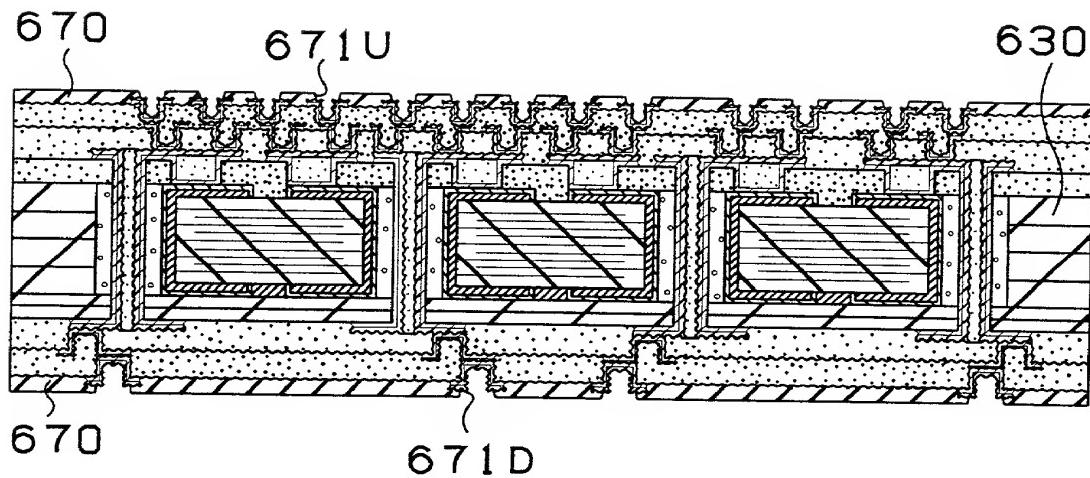
(B)



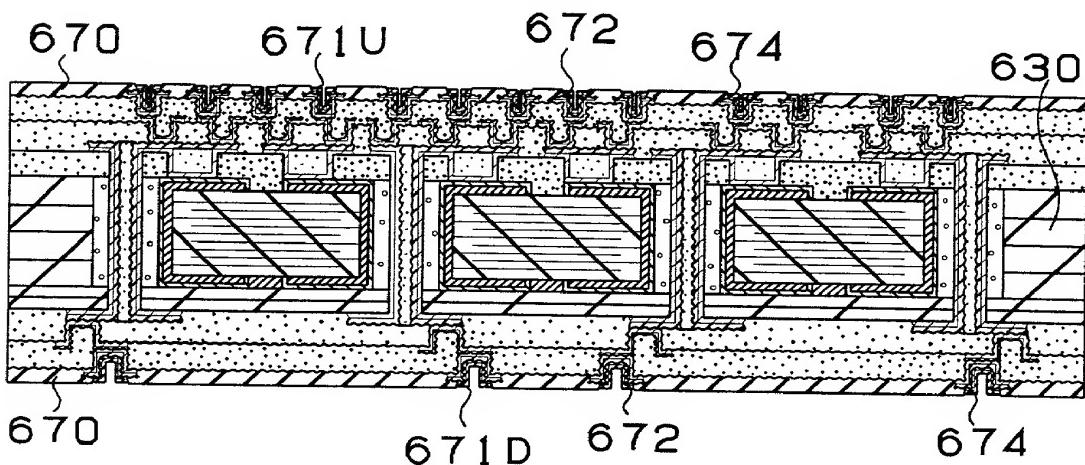
09/830360

51/53  
Fig. 51

(A)



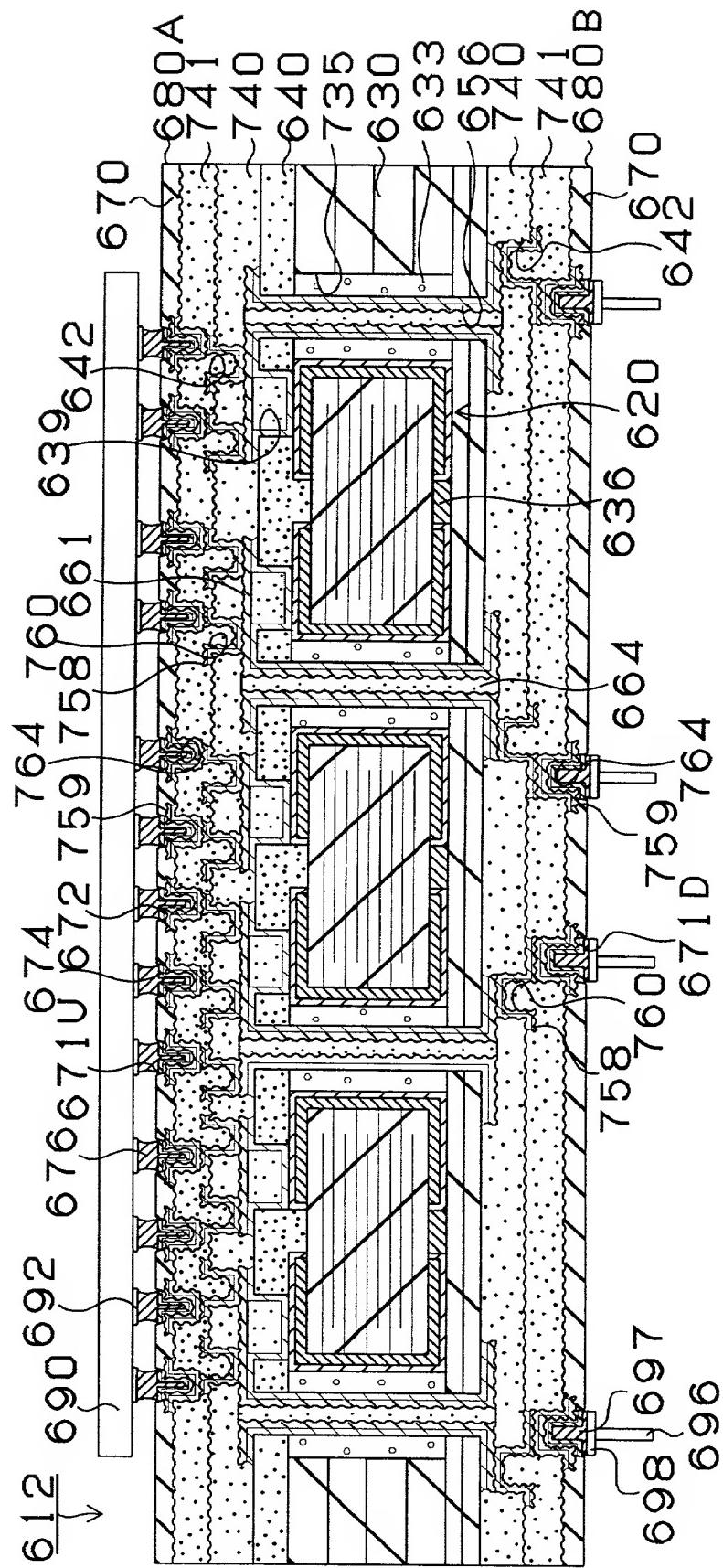
(B)



09/830360 "C14250"

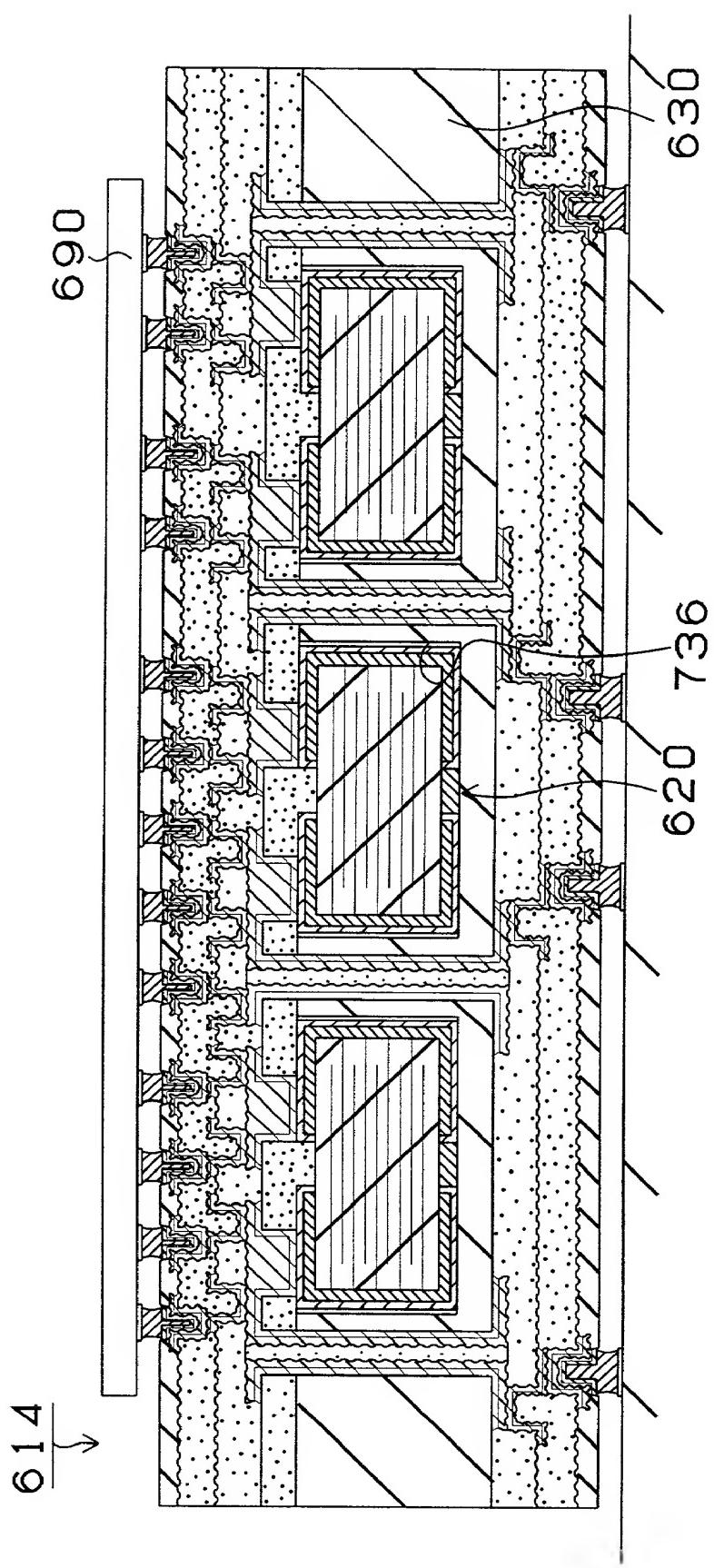
09/830360

Fig. 52  
52/53



09/830360

Fig. 53  
53/53



FOR UTILITY/DESIGN  
CIP/PCT NATIONAL/PLANT  
ORIGINAL/SUBSTITUTE/SUPPLEMENTAL  
DECLARATIONS

RULE 63 (37 C.F.R. 1.63)  
DECLARATION AND POWER OF ATTORNEY  
FOR PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Pillsbury  
Winthrop  
FORM

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the INVENTION ENTITLED

Printed Circuit Board And Method Of Manufacturing Printed Circuit Board

the specification of which (CHECK applicable BOX(ES))

A.  is attached hereto.  
BOX(ES) → B.  was filed on \_\_\_\_\_ as U.S. Application No. \_\_\_\_\_ /  
→ C.  was filed as PCT International Application No. PCT/ JP00/05970 on September 1, 2000

and (if applicable to U.S. or PCT application) was amended on \_\_\_\_\_

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56. Except as noted below, I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International Application which designated at least one other country than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International Application, filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which priority is claimed, or (2) if no priority claimed, before the filing date of this application:

PRIOR FOREIGN APPLICATION(S)

Number	Country	Day/MONTH/Year Filed
11-248311	Japan	2/September/1999
11-369003	Japan	27/December/1999
2000-221350	Japan	21/July/2000
2000-230868	Japan	31/July/2000
2000-230869	Japan	31/July/2000
2000-230870	Japan	31/July/2000

Date first Laid-open or Published

Date Patented or Granted

Priority NOT Claimed

If more prior foreign applications, X box at bottom and continue on attached page.

Except as noted below, I hereby claim domestic priority benefit under 35 U.S.C. 119(e) or 120 and/or 365(c) of the indicated United States applications listed below and PCT international applications listed above or below and, if this is a continuation-in-part (CIP) application, insofar as the subject matter disclosed and claimed in this application is in addition to that disclosed in such prior applications, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of each such prior application and the national or PCT international filing date of this application:

PRIOR U.S. PROVISIONAL, NONPROVISIONAL AND/OR PCT APPLICATION(S)

Application No. (series code/serial no.)	Day/MONTH/Year Filed	Status	Priority NOT Claimed
		pending, abandoned, patented	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Pillsbury Winthrop LLP, Intellectual Property Group, 1100 New York Avenue, N.W., Ninth Floor, East Tower, Washington, D.C. 20005-3918, telephone number (202) 861-3000 (to whom all communications are to be directed), and the below-named persons (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, and I hereby authorize them to delete names/numbers below of persons no longer with their firm and to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct the above Firm and/or a below attorney in writing to the contrary.

Paul N. Kokulis	16773	Glenn J. Perry	28458	Stephen C. Glazier	31361	William P. Atkins	38821
Kevin E. Joyce	20508	G. Paul Edgell	24238	Richard H. Zaitlen	27248	Paul L. Sharer	36004
George M. Sirilla	18221	Lynn E. Eccleston	35861	Roger R. Wise	31204	Robin L. Teskin	35030
Donald J. Bird	25323	David A. Jakopin	32995	Michael R. Dwonczyk	36787		
Dale S. Lazar	28872	Mark G. Paulson	30793	W. Patrick Bengtsson	32456		
				Jack S. Barufka	37087		
				Adam R. Hess	41835		

Date: 3/22/2001

(1) INVENTOR'S SIGNATURE: <u>YASUSHI INAGAKI</u>		First	Middle Initial	Family Name
1-00	<u>Yasushi</u>			<u>INAGAKI</u>
Residence	Ibi-gun	JPX	Japan	Japan
City	State/Foreign Country			Country of Citizenship
Mailing Address	c/o Ogaki-kita-kojou, IBIDEN Co., Ltd., 1,Kitakata 1-chome, Ibigawacho, Ibi-gun, Gifu Japan			
(include Zip Code)	501-0695			

(2) INVENTOR'S SIGNATURE: <u>Motoo Asai</u>		First	Middle Initial	Family Name
2-00	<u>Motoo</u>			<u>ASAI</u>
Residence	Ibi-gun	JPX	Japan	Japan
City	State/Foreign Country			Country of Citizenship
Mailing Address	c/o Ogaki-kita-kojou, IBIDEN Co., Ltd., 1,Kitakata 1-chome, Ibigawacho, Ibi-gun, Gifu Japan			
(include Zip Code)	501-0695			

Date: 3/22/2001

"X" box  FOR ADDITIONAL INVENTORS, and proceed on the attached page to list each additional inventor.

See additional foreign priorities on attached page (incorporated herein by reference).

Atty. Dkt. No. PM

(M#)

## DECLARATION AND POWER OF ATTORNEY

(continued)

## ADDITIONAL INVENTORS:

(3) INVENTOR'S SIGNATURE:

*Dongdong Wang*

Date: 3/22/2001

3-00

First		Middle Initial	Family Name
Residence	Ibi-gun, <i>JPX</i>	Japan	Japan
City		State/Foreign Country	
Mailing Address	c/o Ogaki-kita-kojou, IBIDEN Co., Ltd., 1, Kitakata 1-chome, Ibigawacho, Ibi-gun, Gifu Japan		
(include Zip Code)	501-0695		

(4) INVENTOR'S SIGNATURE: *Hideo Yabashi*

Date: 3/22/2001

4-01

First		Middle Initial	Family Name
Residence	Ibi-gun, <i>JPX</i>	Japan	Japan
City		State/Foreign Country	
Mailing Address	c/o Ogaki-kita-kojou, IBIDEN Co., Ltd., 1, Kitakata 1-chome, Ibigawacho, Ibi-gun, Gifu Japan		
(include Zip Code)	501-0695		

(5) INVENTOR'S SIGNATURE:

*Seiji Shirai*

Date: 3/22/2001

5-01

First		Middle Initial	Family Name
Residence	Ibi-gun, <i>JPX</i>	Japan	Japan
City		State/Foreign Country	
Mailing Address	c/o Ogaki-kita-kojou, IBIDEN Co., Ltd., 1, Kitakata 1-chome, Ibigawacho, Ibi-gun, Gifu Japan		
(include Zip Code)	501-0695		